Sentry 400
Computer Controlled Test System
Instruction Manual

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FAIRCHILD
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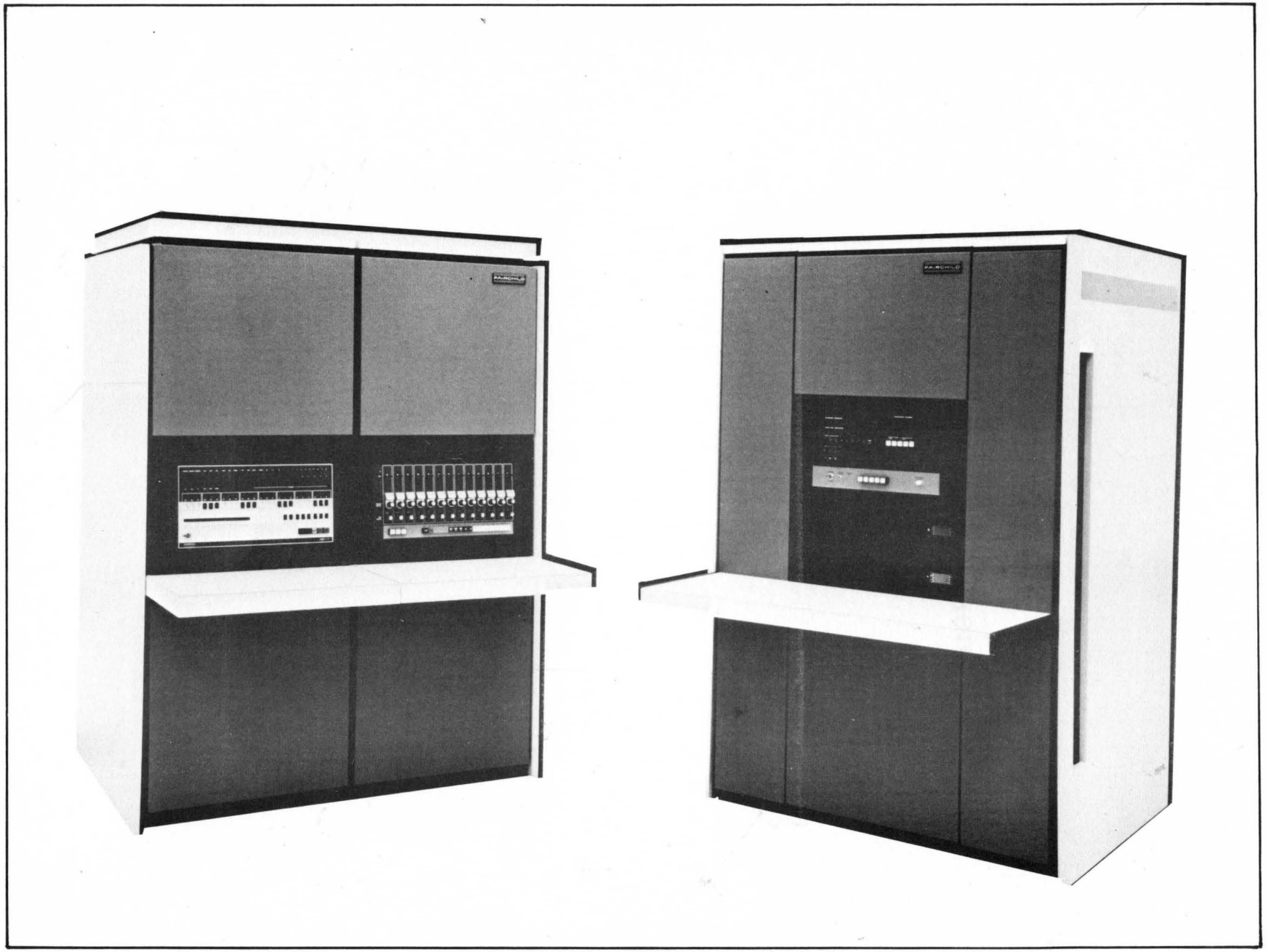

Frontispiece Sentry 400 Computer Controlled Test System.

Section I
General Information

1.1 INTRODUCTION

This manual provides information for installation, operation and programming of the Sentry 400 Computer Controlled Test System. The description in this manual is confined to the tester portion of the system; the FST-1 Fairchild computer and software packages are described in separate manuals. Section I contains a general description of the system together with a table of specifications. The photograph on the facing page is a front view of a single station Sentry 400 Computer Controlled Test System.

1.2 GENERAL DESCRIPTION

The Sentry 400 Computer Controlled Test System provides the capability to automatically test digital networks such as; large scale integrated arrays (MOS, BIPOLAR), complex integrated circuits, printed circuit cards, and other digital subsystems. Multiplexing is provided for operating four test stations with one FST-1 computer. Each test station can test different electronic devices or modules with up to 120 pins. Each test station pin capability is expandable in groups of 30 up to a maximum of 120 pins. Two 120 pin test enclosures may be used for up to a 240 pin test configuration. Each pin has the capability to be defined either as an input pin or an output pin. Through system software it is possible to instruct the tester to perform various operations on the device-under-test such as assign input/output pins, execute tests, indicate Go/No-Go results and print test results.

Basically, the system performs two types of tests; functional tests (that determine whether the device performs the intended logic operations) and precision DC tests (that determine whether component parameters meet device specifications). Functional tests are performed by forcing programmed logic levels on the input pins of the device-under-test and comparing the device outputs with programmed expected outputs. Absolute DC tests allow programmable measurement of network parameters such as saturation voltage and input leakage. In addition, the magnitude of all test system reference voltages and currents such as Go/No-Go thresholds, device supply voltages and functional logic level forcing magnitudes are programmable.

The number of tests required to adequately test an array has a large influence not only on test throughput rate but also on test system configuration. The maximum test rate is approximately 286,000 functional tests per second and 250 DC tests per pin per second. The maximum number of tests that can be performed on a single device without using programming loops, is approximately 130,000. Using loops, programs can be extended to any length.

1.3 TYPICAL SYSTEM CONFIGURATION

Figure 1-1 shows the basic block diagram of the system. The Fairchild FST-1 computer is the primary controller. Tester instructions are held in bulk storage (disc or magnetic tape) and are transmitted to the computer memory when required. The test head, power supplies and timing controls receive their instructions from core memory under control of the computer.

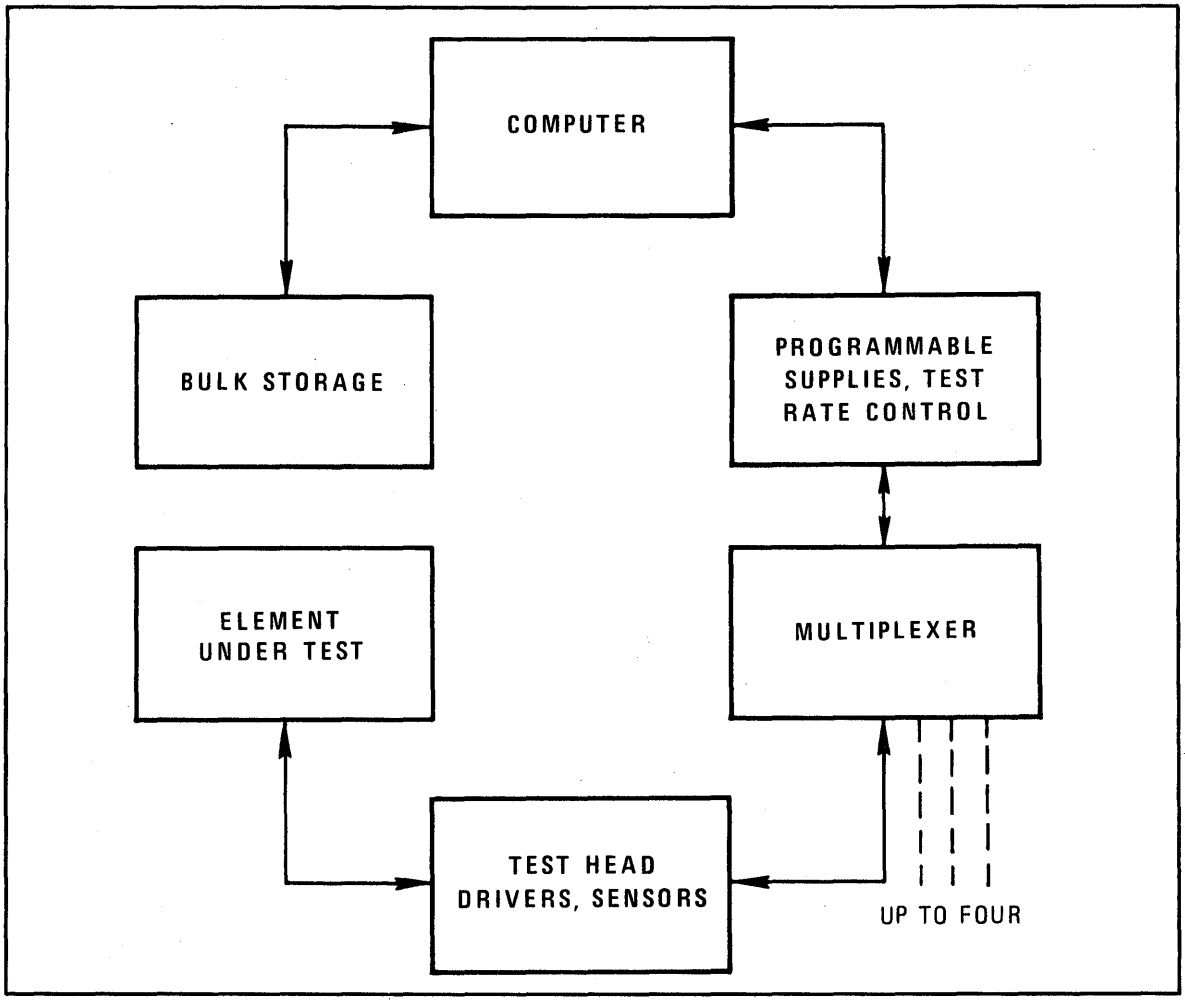

Figure 1-1. Functional Block Diagram

For functional tests, the tester applies logic levels representing forcing functions to the input pins of the unit under test and compares actual outputs to the predicted responses on a "Go/No-Go" basis. The expected output thresholds are programmable as are the input logic levels.

For DC tests, a single pin can be addressed with an instruction that calls for a DC (Absolute) measurement. A switching network then connects the Precision Measurement Unit to the addressed pin and executes the measurement. A pin is always restored to its previous functional test condition prior to being connected to, or released from, the DC measurement unit.

The computer can control the unit-under-test device handler such that wafer indexing and "class" sorting is automatic, depending on the result of tests performed. A fifteen bit storage register is available for this purpose.

Figure 1-2 shows a Sentry 400 test system with multiple test stations. The configuration allows independent testing of devices of different design, therefore increasing the testing throughput rate. The amount of peripheral equipment required per system varies according to the environment of operation. For example, test engineering may require the most peripherals since these groups will be continually generating new-design test programs and new test techniques. The operations are typical electronic data processing operations and are most efficiently done only if a card reader, magnetic tape, disc, printer, and teletype are available. In the production wafer-test environment, a minimum of peripherals are required. Prepared programs on magnetic tape can easily be transferred to the disc. There can be 350 programs of an average length of 1450 tests stored on the disc for immediate access. Figure 1-3 shows probable peripheral configurations for the engineering, wafer-test, and package test systems.

1.4 TESTER OPERATING FEATURES

There are three basic modes of operation for the test system: (1) Automatic, (2) Manual, (3) Monitor.

1.4.1 Automatic

In the Automatic mode the test system operation is self-contained within the program. This mode of operation is primarily intended for the production environment where there is little need for operator intervention.

1.4.2 Manual

In the Manual mode a single programmed instruction is executed each time the "start" button is depressed. This mode of operation is useful for program verification where the operator needs to single step through a program.

With a multiple test system, any or all stations may be in Manual operation simultaneously. A manual station will not inhibit other stations from testing. After executing a single step at Station A, the controller will accept start requests from other stations before returning to Station A.

1.4.3 Monitor

In the Monitor mode the operator is provided the opportunity to intervene with the programmed control of the test system. This mode is primarily intended for use in the prototype design test environment. In this mode the operator has a variety of options such as, modifying programmed delays, selecting datalogging conditions, modifying programmed voltages, etc. (Voltages may be modified in any mode by the control panel override.)

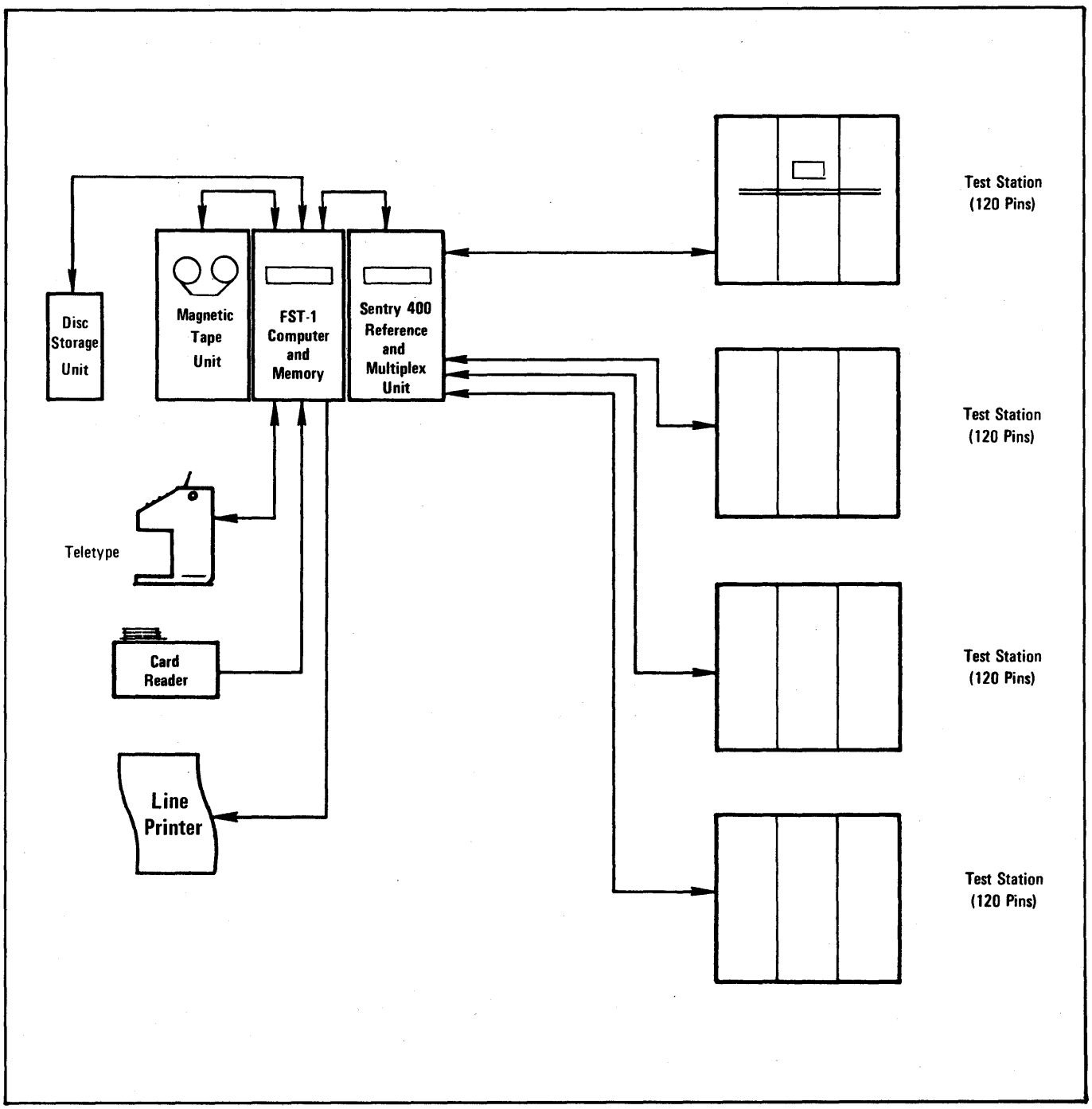

Figure 1-2. Sentry 400 Multiple Test Stations (Maximum Configuration)

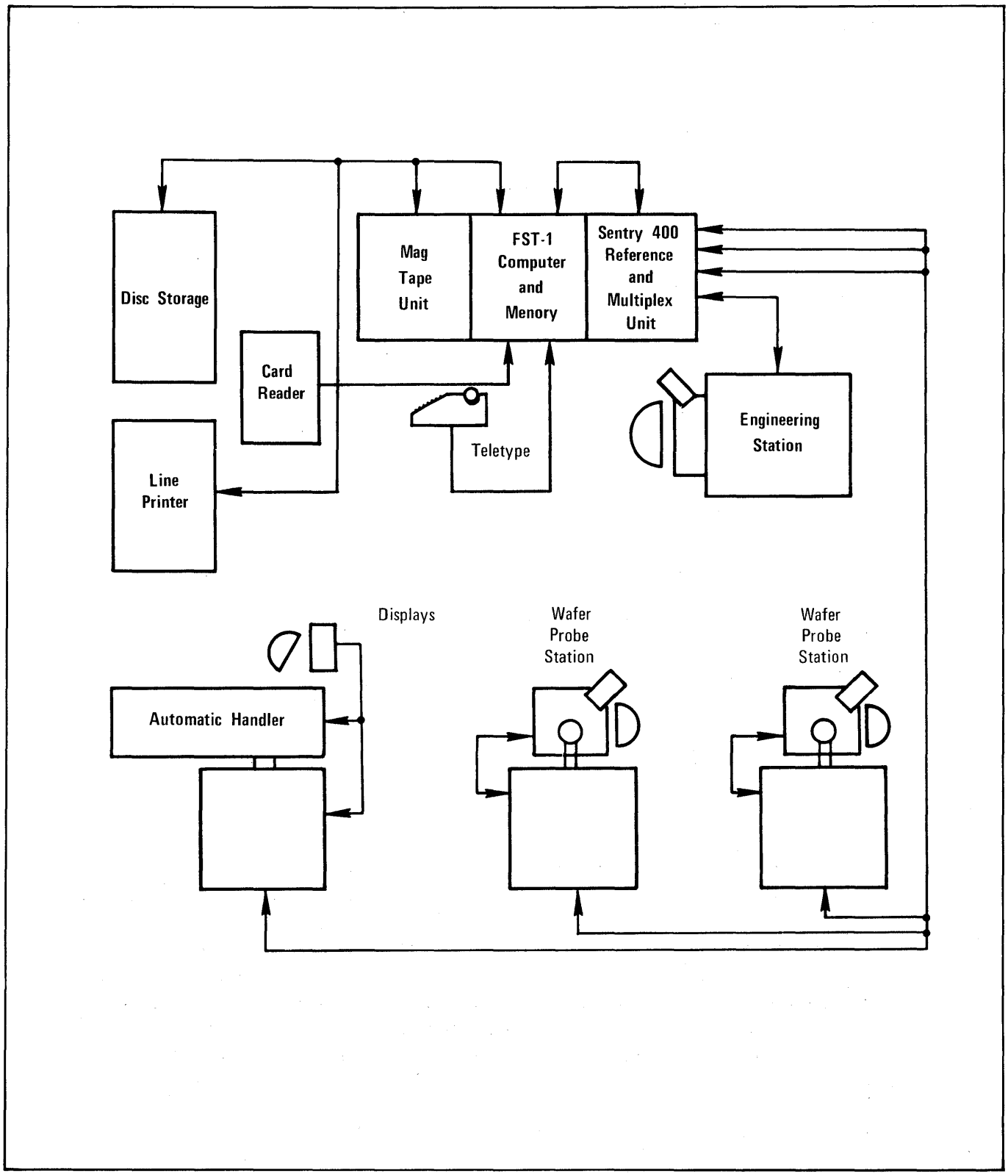

Figure 1-3 Engineering Wafer-Test and Package Test Systems

When the monitor switch is on, and TOPSY is resident in core, the operator can instruct the tester to perform functions that are primarily useful while debugging a prototype array. Examples of these instructions are listed below:

1. Title message (date, run number, etc.).
2. Stop on failure.
3. Stop on instruction Number N.
4. Modify the test rate.
5. Recycle on a group of functional tests. This allows the element-under-test response wave forms, to be displayed on an oscilloscope.
6. Datalog on functional failure.
7. Datalog DC parameter failures.
8. Datalog any measurement so specified in the program.
9. Datalog all functions listed above.
10. Specify test programs on respective test stations.
11. Sync on instruction Number N to trigger some external monitoring device when the program executes Statement N.
12. Specify values of global variables.

1.4.4 Timing

The tester timing with respect to the element-under-test can be programmed such that either combinatorial or sequential networks can be readily tested. For functional tests on combinatorial networks the tester comparator "strobe" is delayed according to the programmed test rate counter. For functional tests on sequential networks there are sync signals available on ~~a front panel jack~~ the first load board which can be wired to the clock pins on the element-under-test. Alternatively they can be wired to wave shaping circuits (supplied by the user) and then to the element-under-test, or can be used to trigger external clock generators. The timing for sequential tests supplies a minimum of one sync pulse followed by a "strobe" to the comparators. The "strobe" is delayed according to the programmed test rate.

1.5 SENTRY 400 SYSTEM DESCRIPTION

The Sentry 400 System consists of a single bay enclosing each test station and a double bay enclosing the FST-1 Computer and Monitor Station. A maximum of four test stations may be used in a single installation. The following paragraphs briefly describe the functions of each bay.

1.5.1 Test Station

Figure 1-4 is an illustration of a test station. Directly below the controls and display panel are the input/output connectors. Each connector provides two terminals (force and sense) for each DUT pin. Pins 1-30 and 31-60 are accommodated by the bottom right and left hand connectors and pins 61-120 are accommodated by the two top connectors. The user may wire his test socket or probe ring to the appropriate pins of the connectors. Five load boards for each 30 pin configuration are provided the user. The load boards, when inserted, are connected in parallel with the appropriate pins of the connector. They may be used in such applications as tests performed with output pins under load, collector outputs requiring pull up resistors, recirculation logic for high speed shift register testing, etc. Connection between the test socket and test circuits are provided by high speed relays. The relays connect either the drivers, detectors, or utility lines to the pins according to programmed instructions.

The controls and display panel contains various controls and indicators that enable the operator to start a test either in the automatic or manual mode of operation. For this purpose a pushbutton labeled MAN is provided. When this pushbutton is depressed the station is in Manual mode. A second button, ADV, enables the operator to single step through a test program. If the MAN pushbutton is not depressed the system is in Automatic mode. Indicator lamps inform the operator of the pass or fail status of the device both for function testing and parameter testing; the end of a test is also displayed. These indicators are updated any time testing pauses.

Register Selector pushbuttons allow the operator to select two long registers whose contents will be simultaneously displayed by two rows of 15 register display lamps. There are eight ranks to each register. By appropriate combination of rank selector and register selector the status of all 120 pins can be displayed.

The rank fail indicator illuminates when a pin of a certain rank fails. This register may then be displayed on the register display lamps to determine which pin has failed. This type of display is useful while debugging prototype designs and test program verification. Input/output pin assignments can be displayed on one row while the forcing and expected outputs are displayed on the other row. The selector switches also allow the comparator register mask (ignored pins), utility and input reference select registers to be displayed. The selector switch will also enable a lamp test.

There is a numerical display of the test instruction number which is currently in the tester. This is extremely valuable for program verification by the operator when the tester is in the manual mode and is being single stepped. It is always updated with the number of the last test executed when the test pauses.

A Precision Measurement Unit is provided for each test station to measure the DC characteristics of the pins of the device-under-test. This type of testing is essential for specifying semiconductor parameters such as saturation voltage and input leakage. The Precision Measurement Unit is capable of forcing a voltage or current on any tester pin. The Precision Measurement Unit also is capable of measuring internal test head analog reference voltages and power supply voltages and currents for purposes of system self-check under program

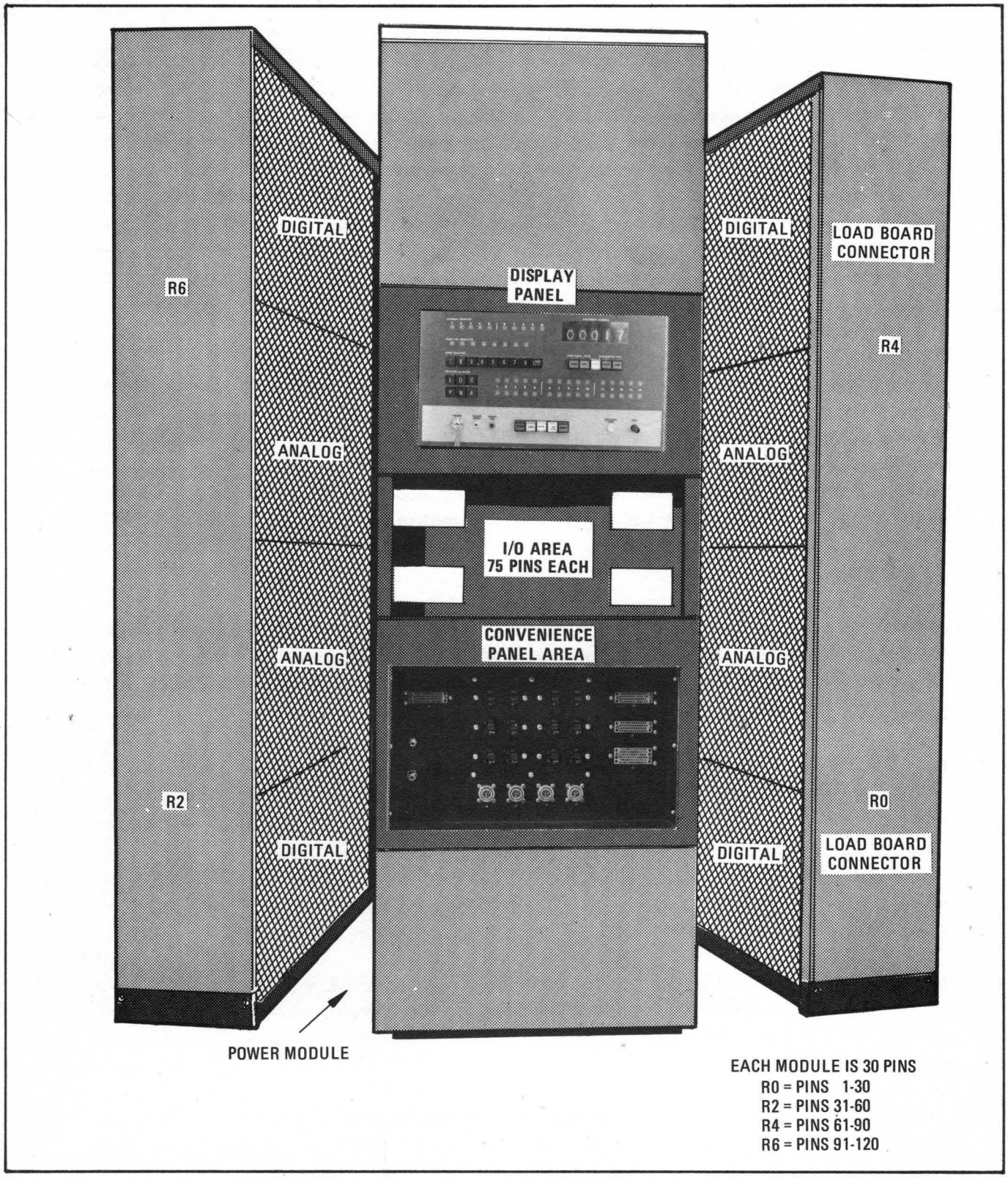

Figure 1-4. Sentry 400 Test Station

control. Measurements are made with a high speed analog-to-digital converter with a 0.1% accuracy and resolutions for voltages from 1 millivolt to 40 volts in three ranges and currents from 1 nanoampere to 100 milliamperes in four ranges.

The mechanical configuration of the test station is designed not only for ease in operation but also from the servicing and expansion point of view.

The control panel is hinged on the bottom; slight forward pressure on the top of the panel will release the front panel and reveal the display lamps and circuitry associated with the controls and indicators. The complete control and indicator module may be removed by removing two thumb screws and a single connector at the rear of the module.

The power supplies are contained in the center section of the bay, and are accessible by pulling on the black handle recessed in the side door frames. The power supplies are mounted such that all potentiometer controls are available for adjustment. The side door frame members contain all the connectors into which are inserted printed circuit cards, containing drivers, detectors, and logic circuits.

A convenience panel located below the working surface, provides 115 volts ac convenience outlets, connectors for handlers, wafer probes, external clock pulses, vacuum and air outlets and connectors for foot operated switches.

1.5.2 Monitor Station

Figure 1-5 is an illustration of the Monitor Station and FST-1 Computer. The monitor station is contained in the right hand half of the double bay. All digital programmable supplies and Reference Voltage supplies are contained in this bay. The main function of this station is to provide manual adjustments of all DPS's and RVS's. Selector switches enable the operator to select a test station for monitor operation; all other stations continue normal operation under program control.

Coarse and fine adjustments permit the operator to manually override the programmed voltages of the DPS's or RVS's. The voltages may be displayed on a Nixie light display provided by a digital voltmeter. Many of the advantages and features of the monitor station are described in the Tester Operating Features section of this manual.

The control panel, like the test station, is hinged and can be folded down. The control panel and chassis is mounted on runners and can be pulled forward revealing a vertical chassis which in turn is hinged at the rear and can be folded back. All DPS's and RVS's and control circuits are mounted on plug-in boards and mounted in the vertical foldout chassis. The main power distribution module for the entire Sentry 400 System is contained in the rear of the monitor station main frame. Two 208 volts, AC, five-wire inputs are filtered and distributed at the required voltage levels to the system. Power for the monitor station is provided by six supplies. Potentiometer adjustments for these supplies are accessed through a power adjustment panel, below the working surface. A power distribution unit (8005) is also available which provides isolation/constant voltage for the Sentry 400 in sub-standard power environments.

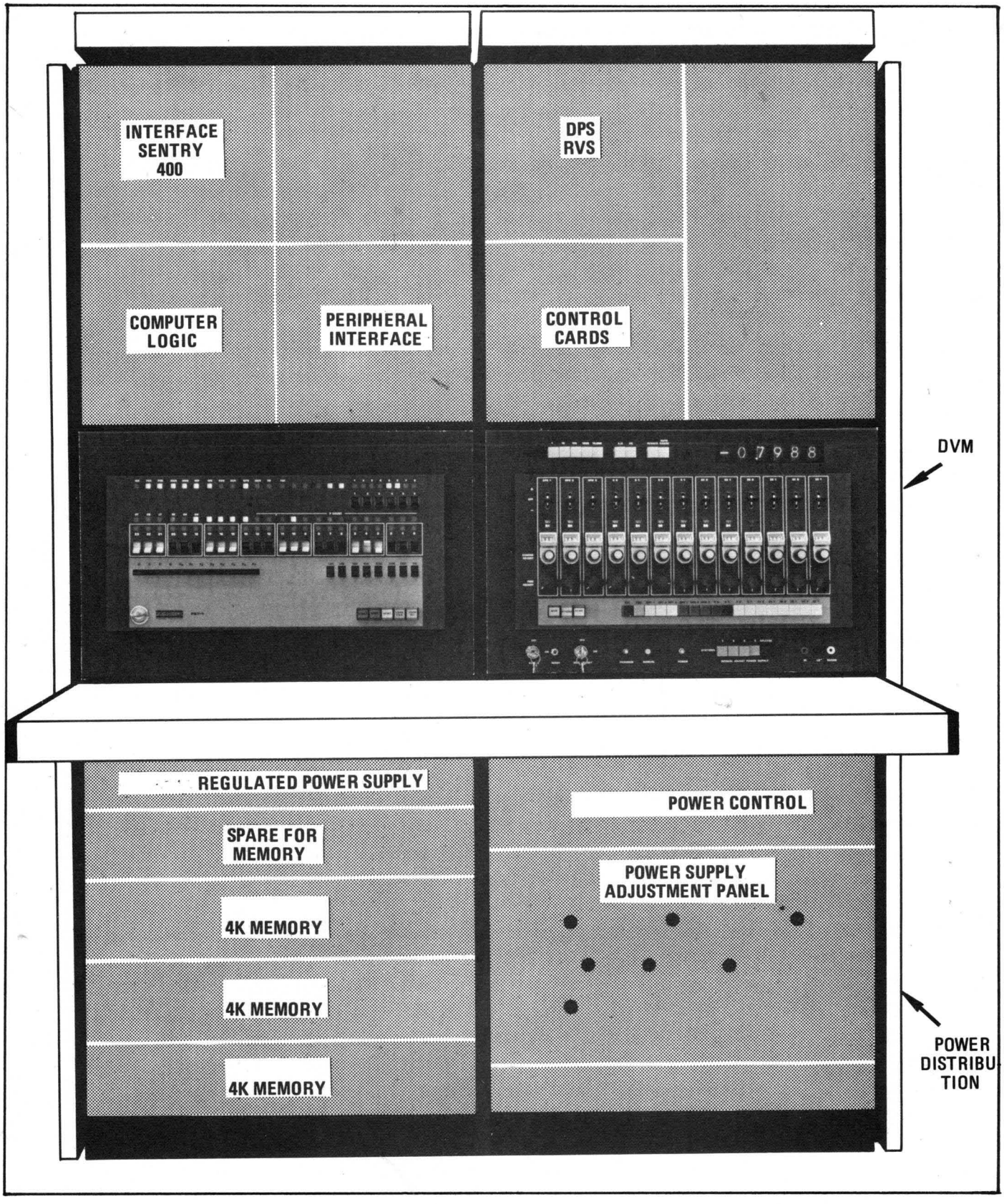

Figure 1-5. Monitor Station and FST-1 Computer

1.5.3 FST-1 Computer System

The FST-1 is a general purpose digital computer occupying the left hand portion of the double bay next to the monitor station (see Figure 1-5). Listed below are some of the FST-1 features:

24-bit data word

1.75 microsecond memory-cycle time

Magnetic ferrite-core memory

4096-word memory modules

Options to comprise a maximum of four memory modules, a total of 16,384 words per CPU

Dual memory-access subsystems via two memory busses

Random direct memory access, stored or retrieved at 571,000 words per second per memory bus

Separate interface control between memory modules and CPU or peripheral units

Interrupt subsystem for communications and datum transfer between CPU and peripheral units via accumulator bus

16 external interrupt channels and a maximum of 63 interrupt locations in memory

Seven index registers for address modification

Indirect addressing for most instructions

A six bit operation code for the following types of instructions:

load and store
arithmetic
logical operations
register and state
conditional and unconditional branch (transfer-of-control)
shift
input/output

Two's-complement single and double precision arithmetic—add, subtract, and hardware multiply and divide.

The FST-1 Computer System basically consists of three subsystems; the central processing unit, memory and interface. The two memory modules (third and fourth optional) providing 4096

word locations each are contained in the bottom half of the bay below the controls and indicator panel. The CPU and interface are contained on the same chassis as the front panel. The front panel and chassis are mounted on runners and when pulled out, reveal the locations of the CPU and interface. The area generally is divided into four groups, A1, A2, A3, and A4. A1 contains the CPU, A2 contains Sentry 400 system interface, A3 and A4 contain the peripheral unit interface.

All controls and indicators for the FST-1 are contained on the front panel. The switch register switches provide a means of manually setting up a 24 bit word, where a switch in the up position represents a binary "1" and down a binary "0." The contents of the registers are displayed by display lamps located above each switch.

The contents of various other working registers may also be displayed on the display lamps by means of switches in the lower left portion of the panel. In the bottom right hand are located the main computer switches; i.e., START, STOP, etc. A group of indicators display the peripheral status of the various input/output units that interface with the CPU.

The basic configuration for the FST-1 is shown in Figure 1-6. Data is held in the disc file and on demand transferred to the memory.

The A memory and B memory data buses are interfaced to the memory and are primarily used for transmitting functional test data at memory speeds to and from the tester and computer peripherals. Both of these memory buses may be in operation simultaneously providing they are communicating with two different peripherals. For instance; the B memory could be transferring function test data to the tester, and simultaneously the disc file could be transferring new test programs to memory. Access to memory is decided on a priority basis.

The accumulator bus is interfaced to the CPU and is used for controlling the digital-to-analog and analog-to-digital converter subsystems. Systems falling into this group include the Digital Programmable Power Supplies, Reference Voltage Supplies, Output Pin Reference Supplies and data to the Precision Measurement Unit. The accumulator bus is also used for communicating tester status, mode and interrupt information. A large and comprehensive software package is provided by Fairchild for controlling the system. The Disc OPerating SYstem program (DOPSY) is used for controlling data to and from the disc and memory. The Tester OPerating SYstem (TOPSY) is used for controlling program transfer between memory and the tester; FACTOR (Fairchild Algorithmic Compiler Tester ORiented) language is very similar to FORTRAN and ALGOL-60 and used as the computer programming language. Various other subroutine library and diagnostic programs complete the software package.

1.6 FUNCTIONAL DESCRIPTION

Figure 1-7 is a simplified block diagram of the Sentry 400 tester circuitry associated with one pin. A minimum system consists of 30 pins worth of circuitry. Additions to the system are made in groups of 30 up to a maximum of 120 pins. For a 240 pin configuration two 120 pin enclosures are used. The driver and detector associated with each pin enables each pin to

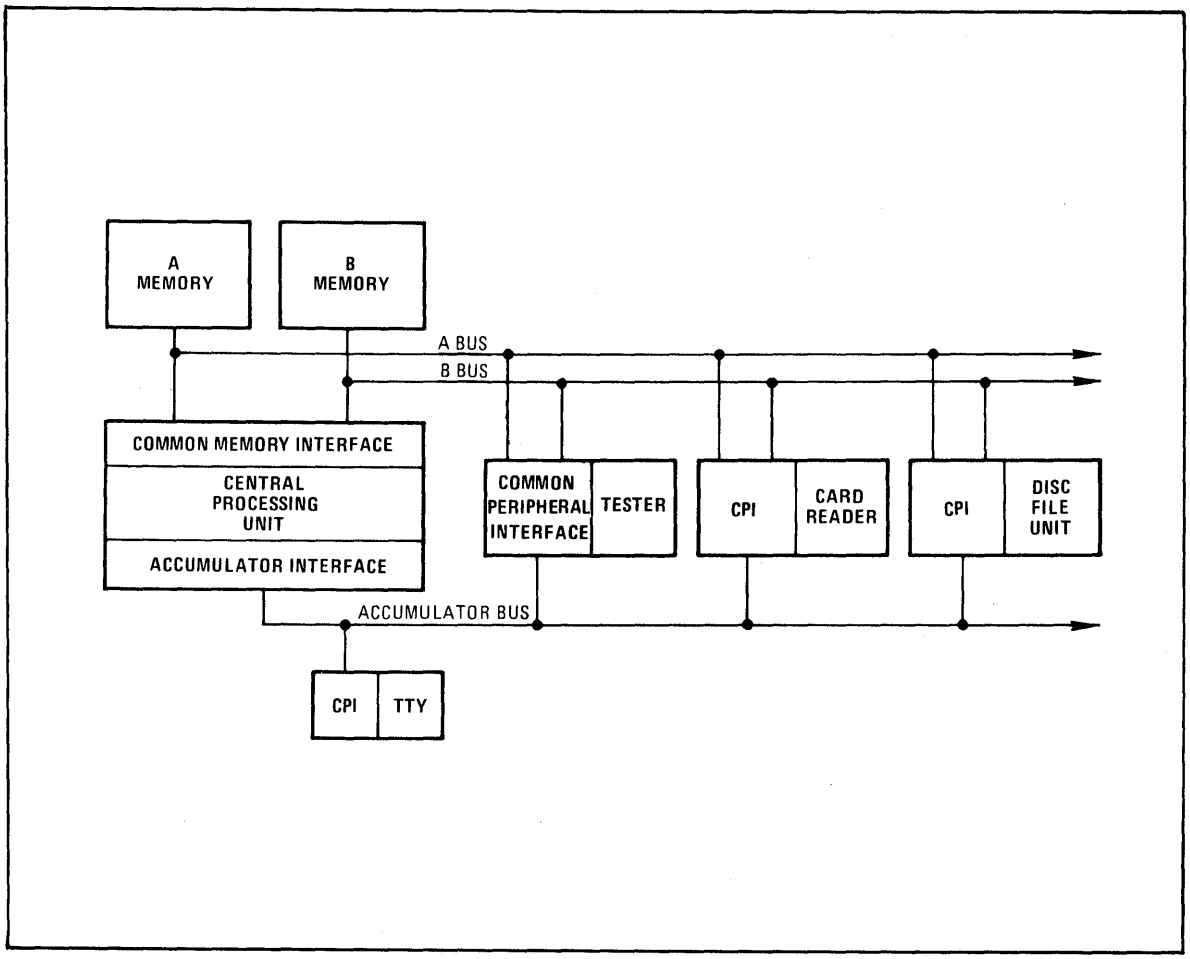

Figure 1-6. FST-1 Computer System, Simplified

be considered as an input pin, an output pin, or both depending upon programming of the registers.

The system is provided with two pairs of analog input references, so that the programmer has the flexibility of choosing between two levels. One of the two input analog buses is selected by a "1" bit in the "S" register. Depending upon the excitation bit in the "F" register, the driver is gated to produce a voltage equal to either the "1" or "0" level of the pair selected by the "S" register.

If the device pin is an input pin a "1" bit in the "D" register closes relay R1. The output of the driver is applied to the pin of the DUT. If the device pin is an output pin a "0" bit in the "D" register opens relay R1. The pin of the DUT is now connected only to the input of the detector. The detector also receives as an input a level proportional to the expected output. If the device pin is an output, the expected output is compared with the actual output of the pin. If the inputs are within the programmed limits, the detector will provide a "0" output that is interpreted as a pass condition. If no comparison exists the detector will provide a "1" output that is interpreted as a fail condition. The detectors are always connected to the sense line through R0 except when the PMU is addressed to that pin. The level on a pin can therefore be sensed whether it be an input pin or an output pin.

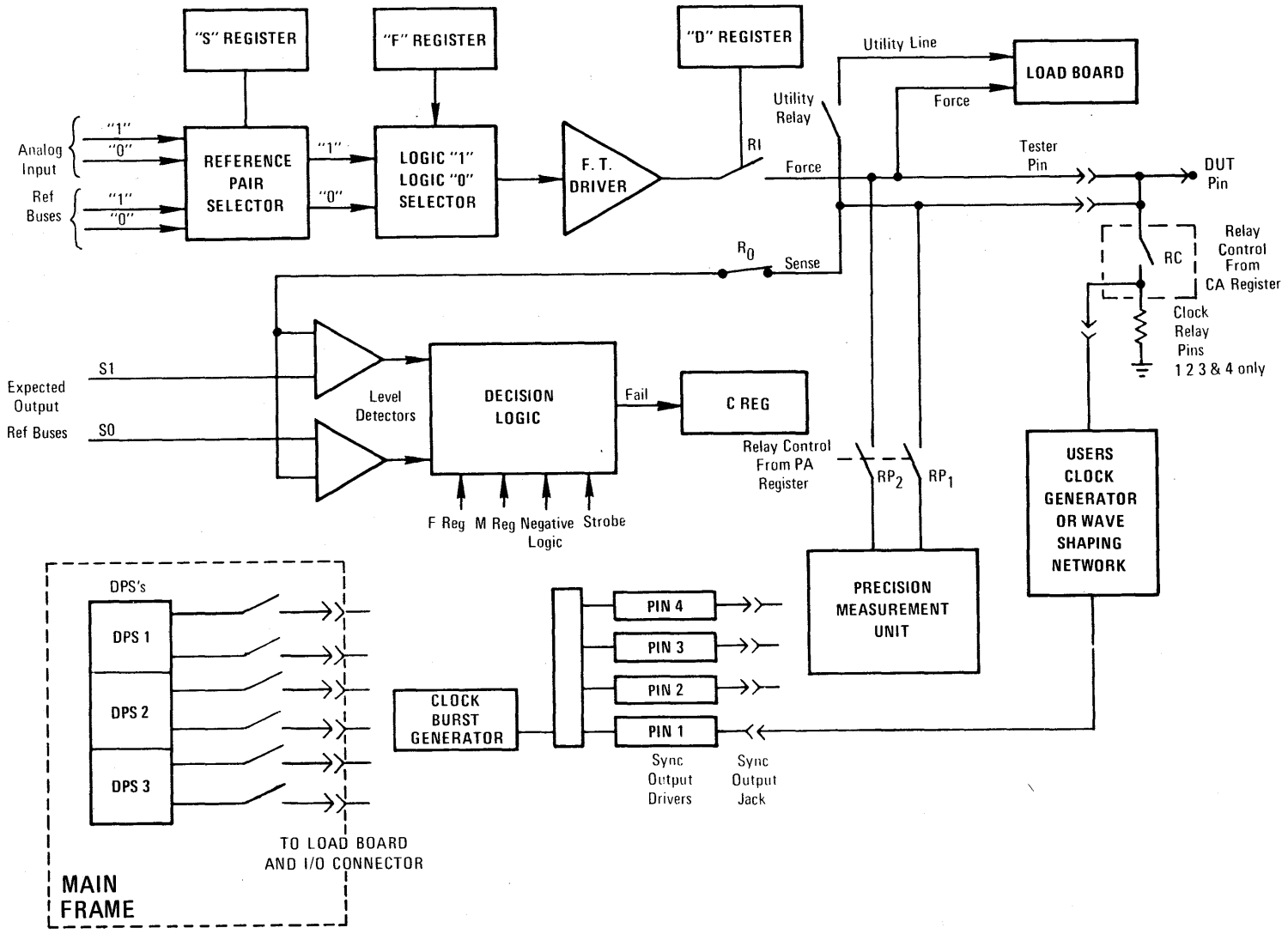

Figure 1-7. Sentry 400 Test Station Block Diagram — Simplified

The detector also receives an input from the M register (mask register). If the programmer is interested in the output, the "M" register is programmed as a "1." The "1" condition enables the detector to make the comparison between the actual output and the expected output. If the programmer is not interested in the output level of the pin the "M" regsiter is programmed as a "0." The "0" condition inhibits the output of the detector. The "C" register and the function test fail output will indicate a pass. This feature is incorporated to prevent unnecessary fail indications on a input pin, or an output pin with an undefined logic state.

1.6.1 Multiplexing

The four test stations will initiate a test program by issuing a START request. Start requests from all stations are stored in the Test Station Control (TSC) register which is located in the mainframe.

At the completion of any station's test program, the tester operating system will read the TSC register via the short register data bus. The Tester OPerating SYstem (TOPSY) sequentially scans the four stations to find a start request. When the software pointer coincides with a start request in the TSC register, the appropriate test head address (two bit code) will be issued and written into the TSC register. The test station address is hardware decoded and one test head enable line (THEN) will become active. This signal resets the station's start flip-flop in the TSC register and connects the long register data and analog buses to the test station addressed.

A test program for each test station will be specified via the teletype monitor commands. When a given test station is enabled, the appropriate test program is loaded from the disc and then executed. At the end of test, the software pointer will start scanning all stations for a start request. The pointer will stop at the next start request received. If the next start request is from the same station that just completed a test, the test program is already resident in main memory and won't be reloaded from the disc. Also, the multiplexer will maintain connection to that test station. If the next start request was from a different test station, and a different test program is being used at that station, then loading of the new program from the disc will be executed and the multiplexer will connect the long register data and analog buses to the addressed station. The whole sequence takes about 30-40 milliseconds maximum.

There is no test station "priority." However, access is not necessarily granted on a first-come first-served basis. Consider this example. Assume the software pointer moves in the 4-3-2-1-4 sequence, and a test at station one is in process. Start requests from stations 2, 3, and 4 that arrive in any order while station one is testing, will be serviced in order 4-3-2.

1.6.2 Manual Mode

Service of test stations in manual mode is handled as follows. The auto/manual switch at each test station controls a bit in the TSC register. When the tester operating system reads the TSC register, and a station with start request on and manual on is selected, the operating system allows one instruction to be executed. Then the TSC register is read and the software pointer scans the start request bits. If no other station issues a start request before

the manual station sends start, the manual station's next start request, will cause another instruction to be executed. Following each instruction executed at the manual station, the operating system scans other stations to see if a start request has been sent. This procedure prevents a station in manual mode from holding up testing at other stations. Therefore, if none of the other stations ever send a start request, the manual station can keep executing instructions without being interrupted. After each manual instruction, the operating system reads the Instruction Number Counter via the short register data bus, and writes the number into the test station Statement Number Display Register via the long register data bus.

Whenever another station issues a start request, the manual station will be interrupted. The operating system will record the number of the last statement executed by the manual station, reset all short registers in the mainframe (except TSC) and issue the address of the new test station. The multiplexer will then connect to the new test station and its program will be executed.

The long registers in the manual station will not be reset so the operator can analyze all long register information at that point in the test program. When the manual station start request is issued again, the test program will be executed automatically under computer control up to the previous stopping point plus one more instruction. Again the TSC register will be scanned for start requests. Thus, in manual mode, one instruction is executed for each start request. The manual station has no priority over any other station. If more than one station is in manual, the operating system keeps track of the last statement executed by each station when it becomes interrupted.

A station that is in manual mode and part way through a test program, may change to automatic mode at any time. When start request is issued, the remainder of that test program will be executed automatically.

1.6.3 Output Pin Loading

Output pins can be loaded by either of the following methods:

(a) Connect a resistive load, R_L in series with the functional test driver and the device output pin (the functional test level detector is also connected to the device output pin to allow concurrent Go/No-Go testing). The load current for V_{OH}/V_{OL} is provided by electronically switching the driver reference between EA1 and EA0 according to the output bit in the F register.

(b) Connect a resistive load, R_L to the device output pin in series with a utility relay and one of the programmable power supplies. Load current is then applied when the power supply is programmed to the appropriate voltage level.

1.6.4 Power Supply Decoupling

Device power supply pins can be decoupled by connecting a capacitor in series with a utility relay. If it is necessary to perform a precision leakage test on the device supply pin,

the utility relay can be opened prior to connecting the precision measurement unit to the device pin.

1.6.5 MOS Input Pin Stressing

Low energy pulses can be applied to MOS input pins by connecting the user supplied pulse source to input pins via the utility relays. Control for the pulse source is derived from one of the external registers. However, up to 80 volts differential may be obtained from the Sentry 400 DPS supplies.

1.6.6 Input Bias Voltage

Unused power supplies can be connected to device input pins via utility relays to provide bias voltage.

1.7 PROGRAMMING CHARACTERISTICS

The format of the test program language, FACTOR, is reasonably simple to learn, apply and interpret as to its meaning. In many respects the language is very similar to a high level computer procedural language such as FORTRAN or ALGOL. The FACTOR language provides the following general features:

1. Conditional and unconditional branching.
2. Arithmetic and Boolean manipulations.
3. Input/Output of data and control.
4. Variable references.
5. Statement labels.
6. Procedure and functional calls.
7. Tester statements.

Following are some typical programming statements. These demonstrate some of the features described above.

```
LAB1:   ON FCT, ABORT;
        ON DCT, ABORT;
        ENABLE DCT1 GT 2E-6 AMPS;
        ENABLE DCT0 LT-2E-3 AMPS;
        SET PMU SENSE, AUTO;

LAB2:   SET PMU FORCEV, RNG2; N = 3;
```

```
DCTEST:  FORCE PMU 3 VOLTS; CPMU PIN N;
         MEASURE VALUE; ILEAK = VALUE; FORCE PMU 0 VOLTS;
         MEASURE VALUE; IFWD = VALUE;
         N=N-1;
         IF N NEQ 0 THEN GO TO DCTEST;

FTEST:   CALL FUNCT;
```

Labels are terminated with colons (:)* and statements are terminated with semi-colons (;). The statements between the labels LAB1 and LAB2 are interpreted as follows:

1. If functional or DC test failure is detected, transfer program control to the statement labeled ABORT.

2. The ENABLE statements establish limits for all subsequent DC measurements resulting from the statement MEASURE. If the measured parameter is greater than 2 microamps or less than -2 milliamps the tester will return DC fail status and transfer control to the statement labeled ABORT.

3. The measuring unit is preset to perform auto-ranging in order to obtain the best resolution, and the forcing function is preset to force a voltage in the range 0 to 10 volts.

The statements between labels LAB2 and FTEST form a loop that executes two DC parameter tests on pins 3, 2, and 1 respectively.

If all three DC tests "pass," the next statement to be executed is a call to execute a procedure which might be a sequence of functional tests.

1.8 PHYSICAL DESCRIPTION AND SPECIFICATIONS

This section describes the main frame, test stations, and FST-1 computer with the various options available. Also included is a brief description of the software, general and electrical specifications and physical dimensions. Figure 1-8 is a system configuration illustration showing the model numbers of the various components and options within the system that are described in the following paragraphs.

*Colons are represented by the 0-8-2 code on punch cards which is the "NUMERIC T" on the IBM 29 punch – not the key labeled :

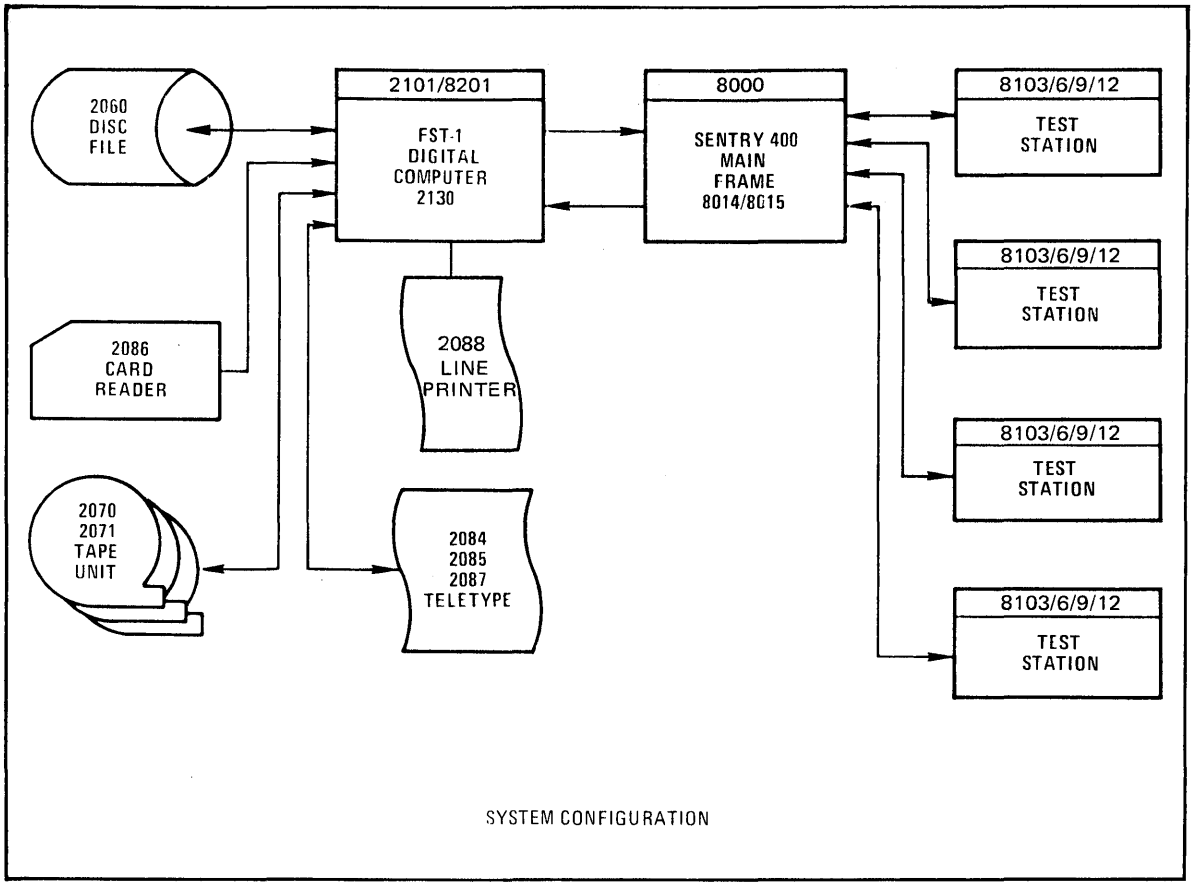

Figure 1-8. System Configuration and Model Numbers

1.8.1 Mainframe and Options

MODEL 8000 SENTRY 400 MAINFRAME, including:

1) Single bay enclosure.

2) AC Power distribution assembly,

3) Monitor control panel.

4) Reference unit power system.

5) Reference and multiplex chassis, including:

–Control logic for Model 8014's and 8015's.
–Multiplex control unit.

6) Interfacing to Model 2101 computer.

MODEL 8014 DUAL REFERENCE SUPPLY. Digitally programmed to provide logical "0" and "1" voltage levels used as references by function drivers and comparators. Three Model 8014 units are required in a basic system to provide two pairs of input reference levels, and a pair of "expected" output comparator levels. Up to two additional 8014's may be used to provide bias levels connected to any device terminal through the Model 8020 load boards, under program control.

MODEL 8015 POWER SUPPLY. Digitally programmed voltage/current source, normally used to provide V_{CC}, V_{DD}, etc.

Programmable voltage or current trip circuitry is included to interrupt system if actual value exceeds programmed trip limit.

Two Model 8015 supplies are recommended in a basic system while one additional unit may be fitted optionally.

MODEL 8020 UNIVERSAL LOAD BOARD. The Model 8020 Universal Load Board as available for the SENTRY 400 system may serve in the following applications:

1) DUT has open collector outputs requiring external pullup resistors.

2) Functional tests are performed with output pins under load.

3) User requires special circuitry to be used under system program control.

Five load boards per each 30 pin module are included in the test stations.

The load boards have patch plugs and receptacles for solderless connection of components.

There are also fifteen address lines for the user to tie to ground or +5 volts to form a board identification code. Thus, the test program can test to see if the correct load boards are inserted.

1.9 TEST STATION

1.9.1 Model 8103, 30-Pin Test Station, including:

1) Standard test station enclosure.

2) Power control module (including isolation filtering and fail monitor).

3) Power supply module.

4) Precision measurement unit.

5) One, 30-pin module of drivers and detectors, including control logic.

6) Station control panel.

7) Five each Model 8020 boards.

1.9.2 Model 8106, 60-Pin Test Station, including:

1) Standard test station enclosure.

2) Power control module (including isolation, filtering and fail monitor).

3) Power supply module.

4) Precision measurement unit.

5) Two 30-pin modules of drivers and detectors, including control logic.

6) Station control panel.

7) Ten each Model 8020 load boards.

1.9.3 Model 8109, 90-Pin Test Station, including:

1) Standard test station enclosure.

2) Power control module (including isolation filtering and fail monitor).

3) Power supply module.

4) Precision measurement unit.

5) Three 30-pin modules of drivers and detectors, including control logic.

6) Station control panel.

7) Fifteen each Model 8020 load boards.

1.9.4 Model 8112, 120-Pin Test Station, including:

1) Standard test station enclosure.

2) Power control module (including isolation filtering and fail monitor).

3) Power supply module.

4) Precision measurement unit.

5) Four 30-pin modules of drivers and detectors, including control logic.

6) Station control panel.

7) Twenty each Model 8020 load boards.

1.10 COMPUTER AND PERIPHERALS

1.10.1 Model 2101 FST-1 Computer, including:

1) Single bay enclosure.

2) CPU logic and power system.

3) 4096 Word (24-bit) core memory.

4) Memory expandable by addition of Model 2130.

5) Computer control panel.

6) 24-bit word length.

7) Full memory cycle time of 1.75 microseconds.

8) Multi-level indirect addressing.

9) Seven hardware index registers.

10) Hardware multiply/divide.

11) Two memory buses provide simultaneous access to two memory banks, via separate DMA channels. Memory data transfer rates in excess of 1 mega-word per second.

1.10.2 Model 2060 Disc File

The disc file is used as a multi-purpose message storage device within the Sentry 400 system. Some of its major applications are:

1) System software storage.

2) Test program storage.

3) Temporary working storage.

4) Data buffer for I/O.

Performance characteristics:

1) Rotation speed: 1745 RPM

2) Access time: 17.8 milliseconds average, 35.5 milliseconds maximum.

3) Data transfer rate: 113,000 words/second.

4) Storage capacity: 768,000 words (24 bit).

The model 2060 includes the controller and interface to the FST-1 computer.

1.10.3 Model 2070 Magnetic Tape Controller

Designed to interface and control up to three Model 2071 magnetic tape transports.

1.10.4 Model 2071 Magnetic Tape Transport

The digital tape memory system is used for a number of applications within the Sentry 400 system. Among these are:

1) Datalogging for subsequent data analysis by FST-1 or off-line computer installation.

2) Large test program library storage.

3) System software storage as back-up for disc file.

4) Data transfer media in multiple system installations, etc.

Performance Characteristics:

1) Tape speed: 24 inches per second.

2) Tape: ½ inch width, 1.5 mil by 2400 feet.

3) Reels: 10½inch IBM or NAB type.

4) Recording density: 800 BPI.

5) Recording format: 9-track ASCII, 0.6 inch IRG (IBM 360-2400 series compatible).

6) Rewind and fast forward speed: 150 IPS.

1.10.5 Model 2121 FST-1 Software Package

The FST-1 computer software package includes the following major components:

ASSEMBLER—Accepts computer programs written in FST-1 assembly language and assembles them into executable object code.

DEBUG–Provides full computer program debugging capabilities.

DOPSY–(Disc OPerating SYstem)

Nonreal time, batch operating disc system. Provides job control, loading, core-allocation and input/output services.

DIAGNOSTICS–Extensive diagnostic package includes programs for automatic checkout of test system electronics, Sentry mainframe electronics, as well as diagnostics for the FST-1 computer instruction set, core memory and peripheral equipment.

1.10.6 Model 2084 Console Typewriter With Paper Tape

The Model 2084 unit consists of a modified ASR-33 Teletypewriter with attached mechanical paper tape reader and punch and interface electronics to the FST-1 computer.

1.10.7 Model 2085 Console Typewriter With Paper Tape

Same as Model 2084 except utilizing heavy duty ASR-35 Teletypewriter.

1.10.8 Model 2087 Console Typewriter

Same as Model 2085 except utilizing KSR-35 Teletypewriter, without paper tape facilities.

1.10.9 Model 2086 Punched Card Reader

The Model 2086 card reader photoelectrically reads standard 80 column punched cards at a rate of up to 200 cards per minute.

1.10.10 Model 2110 Extension Bay

Used to house up to two Model 2071 magnetic tape transports.

1.10.11 Model 2130 Core Memory Expansion

4096 Word (24-bit) module with memory parity.

1.11 SYSTEMS SOFTWARE

1.11.1 Model 8201 Sentry 400 Software Package

The Sentry software package consists of two major components.

These are:

FACTOR–(Fairchild Algorithmic Compiler, Tester Oriented). Allows test programs to be written in a simple, easy to learn "English" like algorithmic language. Generates object code for interpretation and execution by TOPSY. Includes extensive error checking facilities.

TOPSY–(Tester OPerating SYstem). TOPSY is a real time operating system designed to operate the Sentry 400 in its normal mode, testing on-line. The many functions performed and supervised by TOPSY include:

System initialization
Multiplexing
Interrupt Processing
Fetching test instructions
Instruction interpretation
Performance of FACTOR arithmetic operations
Measurement limit comparison
Work stack manipulations
On-line user command processing
Datalogging of test data to selected I/O units.

DIAGNOSTICS–

TDIAG
MDEBUG
VCTST
PMUCAL
A/D
ADCON
DPS

Table 1-1. Electrical Specification Summary

Programmable Unit	Max. No.	Maximum Range	Resolution**	Special Features
Functional Test Driver	120*	±30.72V at ±40mA	10mV/40mV in 2 ranges	Current limits at 50mA, short circuit protected, maximum slew rate 30V/μs.
Functional Test Comparator	120*	±30.72V: 2.5MΩ	10mV/40mV in 2 ranges	Detects open circuit lines, monitors inputs and outputs 0.4μs, response time for 10mV overdrive at -30 to +30V.
Precision Measurement Unit	1*	±40.92V; ±102.3mA	1mV/40mV in 3 ranges 1nA/100μA in 4 ranges	Voltage or current force and sense, programmable current and voltage limit, 100μs A/D converter (11 Bits).
Programmable Power Supply	3	±40.92V; ±1.023A	10mV/40mV in 2 ranges 0.1mA/1mA in 2 ranges	Voltage or current force and sense, Go/No-Go trip output for over or under current or voltage, current/voltage magnitude measurement 1 ms setting time to 1% of full scale.
Programmable Reference	10	±30.72V at ±40mA	10mV/40mV in 2 ranges	Four references for functional test drivers, two for functional test comparators, four for low current bias supplies, 5 ms settling time to 0.1% of full scale.
Time Delay	1	5.73405s	0.35μ/0.35ms in 2 ranges	
Clock-Burst Generator	1	255 sync pulses	1 sync pulse	
Sync Output	4	T^2L Driver 0 to 5V		
Socket Identification		~~32,767~~ codes 4,096 with EN 385-1		

*In one standard test station enclosure, software is configured for up to 240 pins. Two 120 pin test station enclosures are used for a 240 pin tester configuration.

**Accuracy: All forcing and measuring units are accurate to ±1 least significant bit ±0.1% of the value except the PMU 1 microampere and 1 volt ranges which are ±2 LSB and ±0.5%.

Table 1-2. General Specifications

Input Power Requirements	Two five wire three phase inputs at 208V/30A each if the installation consists of more than one test station. For installations with one test station only, one five wire three phase input is required.		
Mainframe Computer Test Station	110Vac at 9A on Phase A 110Vac at 20A on Phase B 110Vac at 20A on Phase C		
Environmental Requirements	+15°C to +30°C, specifications apply at 25°C ±2°C and 50% maximum relative humidity.		
Size	Height	Width	Depth
Mainframe and Computer	66.75"	48"	38"
Test Station	66.75"	42.5"	37.5"
Weight			
Mainframe and Computer Test Station (each)	- ~900 lbs. - varies		
Memory Capacity	Up to four memory banks consisting of 4096, 24 bit words each.		
Type of Tests	Two types of tests. (1) Functional tests, that determine whether the device performs the intended logic operations; (2) DC tests that determine whether component parameters meet device specifications.		
TEST Rate	Maximum 286,000 functional tests per second and 250 DC tests per pin per second. Maximum number of tests that can be performed on a single device is approximately 130,000 without programmed loops.		
TEST STATIONS	Four stations may be multiplexed into the system and controlled by one FST-1 computer. Different device types may be tested at each station in any given mode of operation without affecting testing at other stations.		
Tester Pin Capability	Pin capability is expandable in groups of 30 up to a maximum of 120 pins per test station. Two 120 pin test enclosures are used for a 240 pin configuration.		
Programming Language	FACTOR. (**F**airchild **A**lgorithmic **C**ompiler **T**ester **OR**iented) language. The language is very similar to FORTRAN and ALGOL-60.		
Modes of Operation (1) Automatic	In the automatic mode a complete device program will be performed once the start button is depressed. In the		

Table 1-2. General Specifications (Continued)

	production environment the start pulse is provided by the mechanical handler and the complete program is performed automatically on each device.
(2) Manual	In the manual mode the system will perform a single test of a program each time the start button is depressed.
(3) Monitor	In the monitor mode the operator may intervene with the programmed test and manually modify programmed voltages, test rates, test times, etc. as desired. This mode is ideal for debugging prototype arrays. While in the Monitor mode testing continues uninterrupted at other stations (regardless of mode). The only limitation is that while in the monitor mode data logging on teletype is inhibited.
Software	The system is supplied with a complete software package. Device test programs may be prepared by the user, or, if desired, by Fairchild.
Maintenance	The system-is provided with maintenance routines to help in fault isolation. The hardware has built in self-test capability.

Section II
Installation

2.1 GENERAL

It is Fairchild policy to provide a technical representative to supervise the installation of all Fairchild System Technology products. The following instructions apply to deliveries and installation made under this condition.

2.2 INSPECTION

It is the responsibility of the customer to inspect the crated system before releasing the shipper. Any signs of external damage must be noted by both and called to the attention of the insurance investigator.

2.3 UNCRATING

The customer must not uncrate the system without verbal or written consent from a Fairchild representative. Any external damage discovered during uncrating will be noted and uncrating stopped until the insurance investigator is notified. Do not proceed until so instructed by the insurance investigator. After uncrating, the customer will make a careful inspection to ensure that there is no concealed physical damage to internal electronic circuits or components.

2.4 INSTALLATION

Installation will be made by the customer's staff under direct supervision of a Fairchild representative.

CAUTION

INITIAL POWER MUST NOT BE APPLIED TO THE EQUIPMENT WITHOUT WRITTEN PERMISSION FROM FAIRCHILD.

2.5 RESHIPMENT

When a chassis is damaged in shipping, the insurance investigator can order it returned. The insurance company will assume full responsibility for recrating and reshipment. Neither the customer nor Fairchild are required to assume such responsibility without specific understanding with the insurance company through the proper representative.

When a physically undamaged, unoperational chassis is to be returned, an agreement will be made between Fairchild and the customer as to procedure.

2.6 LAYOUT

Two suggested layouts of the Sentry 400 Test System are illustrated in Figures 2-1 and 2-2. Installation should be such that a 4 foot clearance (minimum) exists at the rear and sides of the bays.

2.7 INTERCONNECTING CABLES

Figure 2-3 is a cabling diagram showing the interconnecting cables for the Sentry 400 Test System and Figure 2-4 shows the interconnecting diagram for the FST-1 computer and peripheral equipment. Caution should be exercised when handling the cables to prevent broken wires, pins and sockets. Test station main frame multiplex and power cable length should be specified and can be up to 50' long allowing a 40' separation between main frame and test station.

2.8 AC POWER

AC power for the system is provided by two five wire 208V/30A three phase inputs. The three phase inputs are connected to J1 and J2 on the rear of the power distribution panel. The three phase input connected to J1 provides power for the main frame (including the FST-1 computer) and test station No. 1. The three phase input connected to J2 provides power for test stations 2, 3 and 4. If the system consists of more than one station both three phase inputs are required. If the system consists of one station input power to J1 only is required. A.C. power for the DISC requires 208 v. single phase 3 wire at 5 amperes.

2.9 AIR CONDITIONING AND HUMIDITY REQUIREMENTS

Environmental requirements are as specified in Table 1-2. General specification: normal room ambient (25°C) at less than 50% relative humidity are ideal conditions. One mainframe and a single test station produces approximately 450 BTU's per minute. Each additional test station produces approximately 170 BTU's per minute. Air conditioning requirements of existing facilities should be modified as required to compensate.

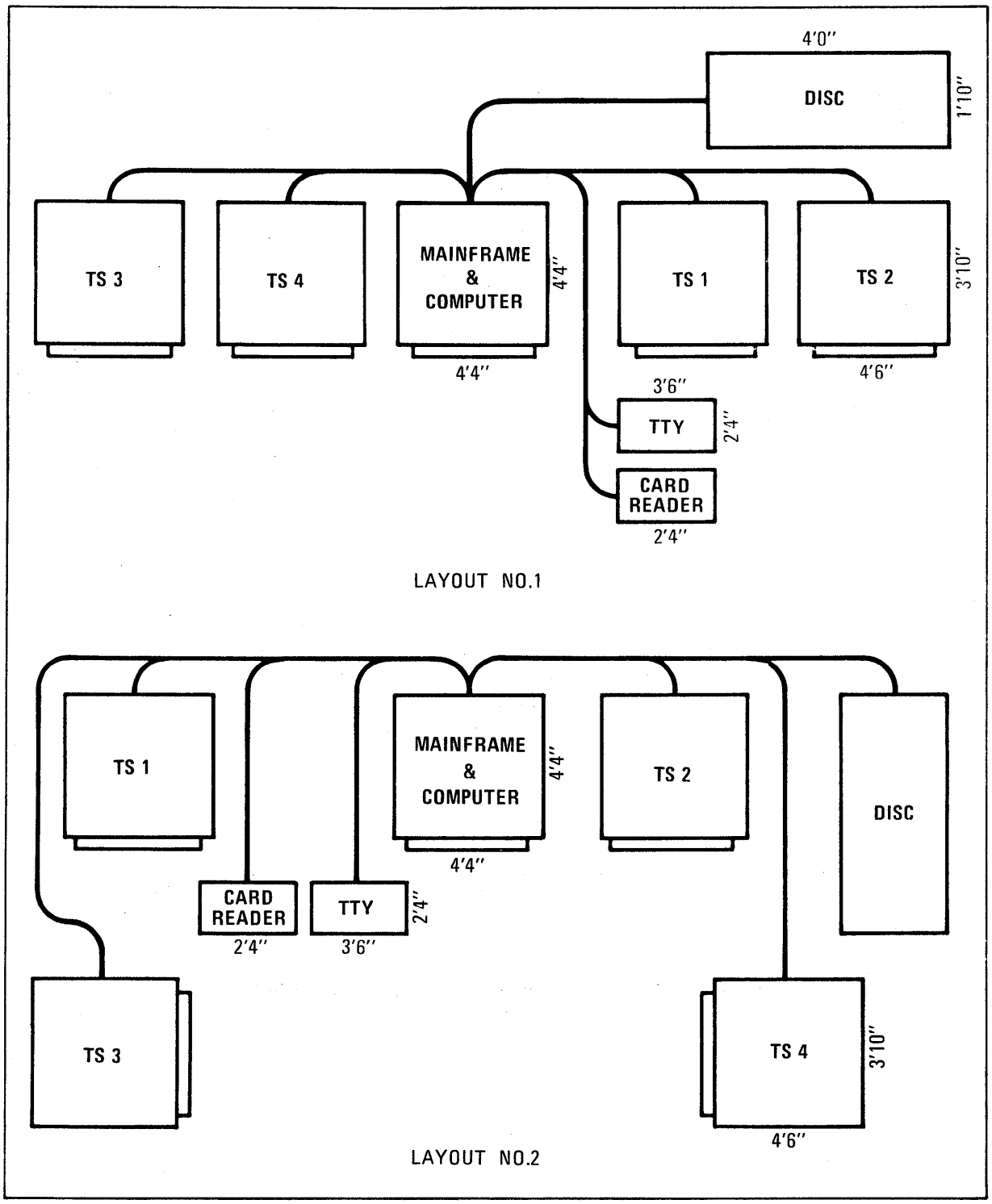

Figure 2-1 Sentry 400 Test System Suggested Layout . . . A

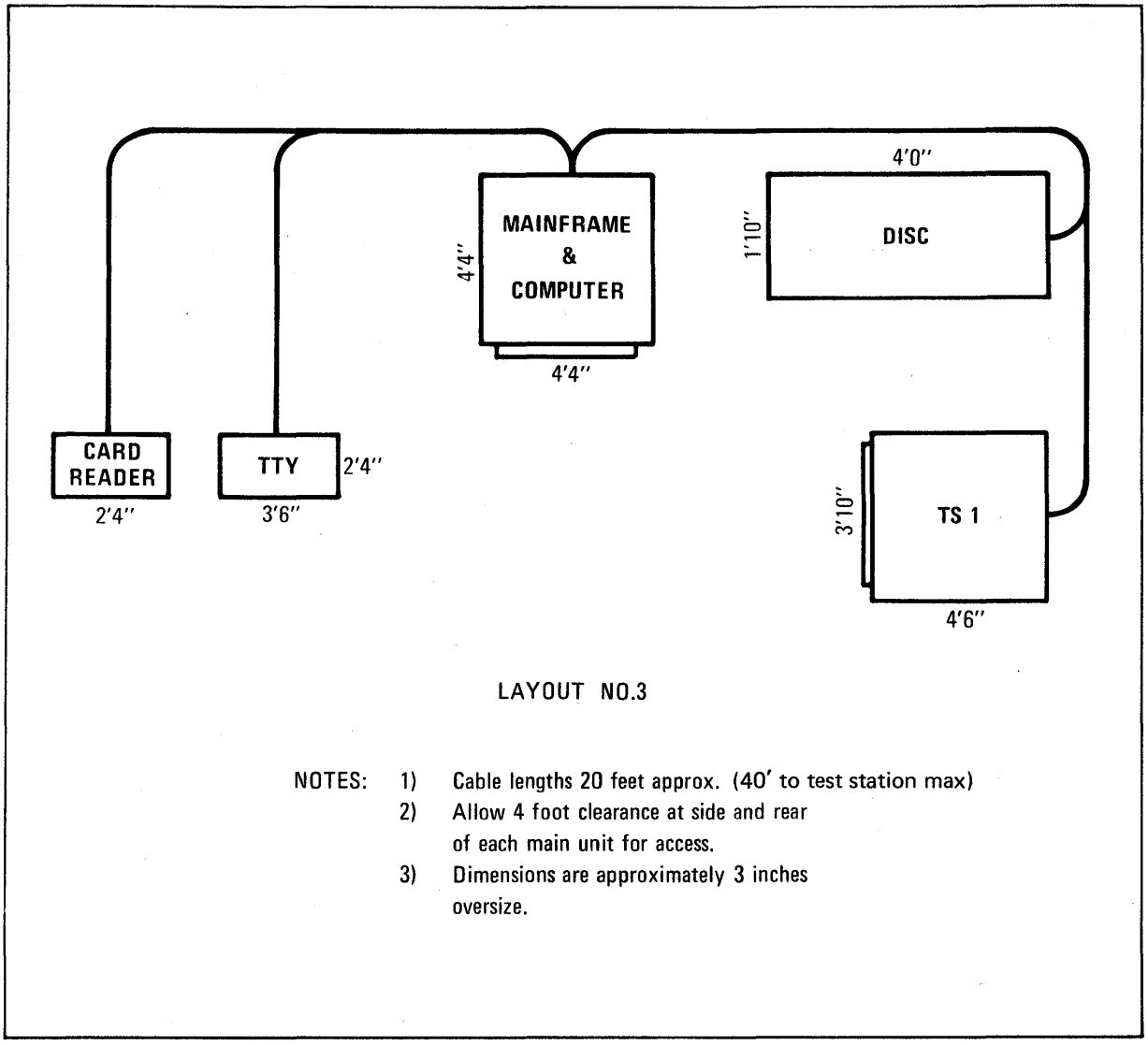

Figure 2-2 Sentry 400 Test System Suggested Layout . . . B

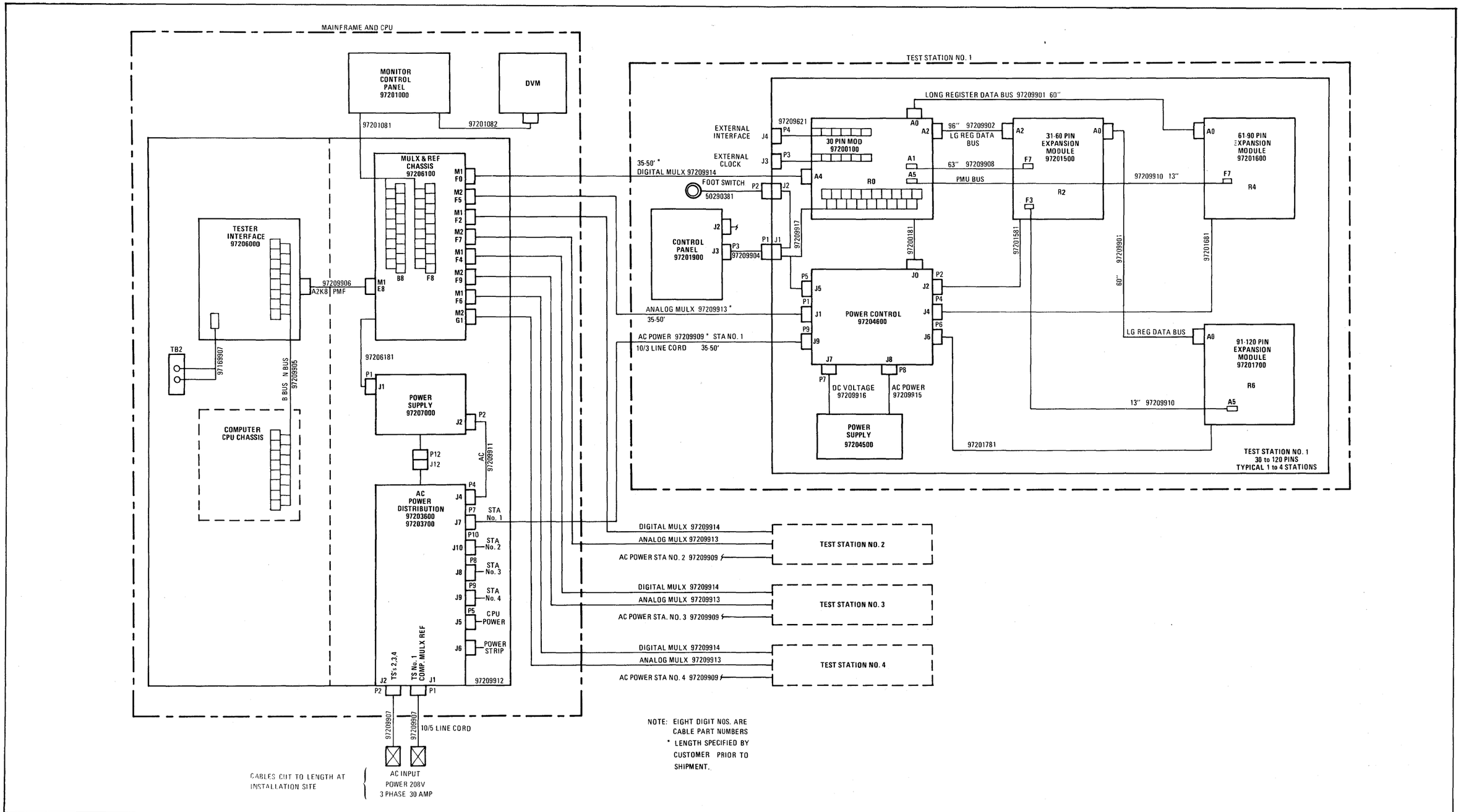

Figure 2-3. Sentry 400 Test System Cabling Diagram

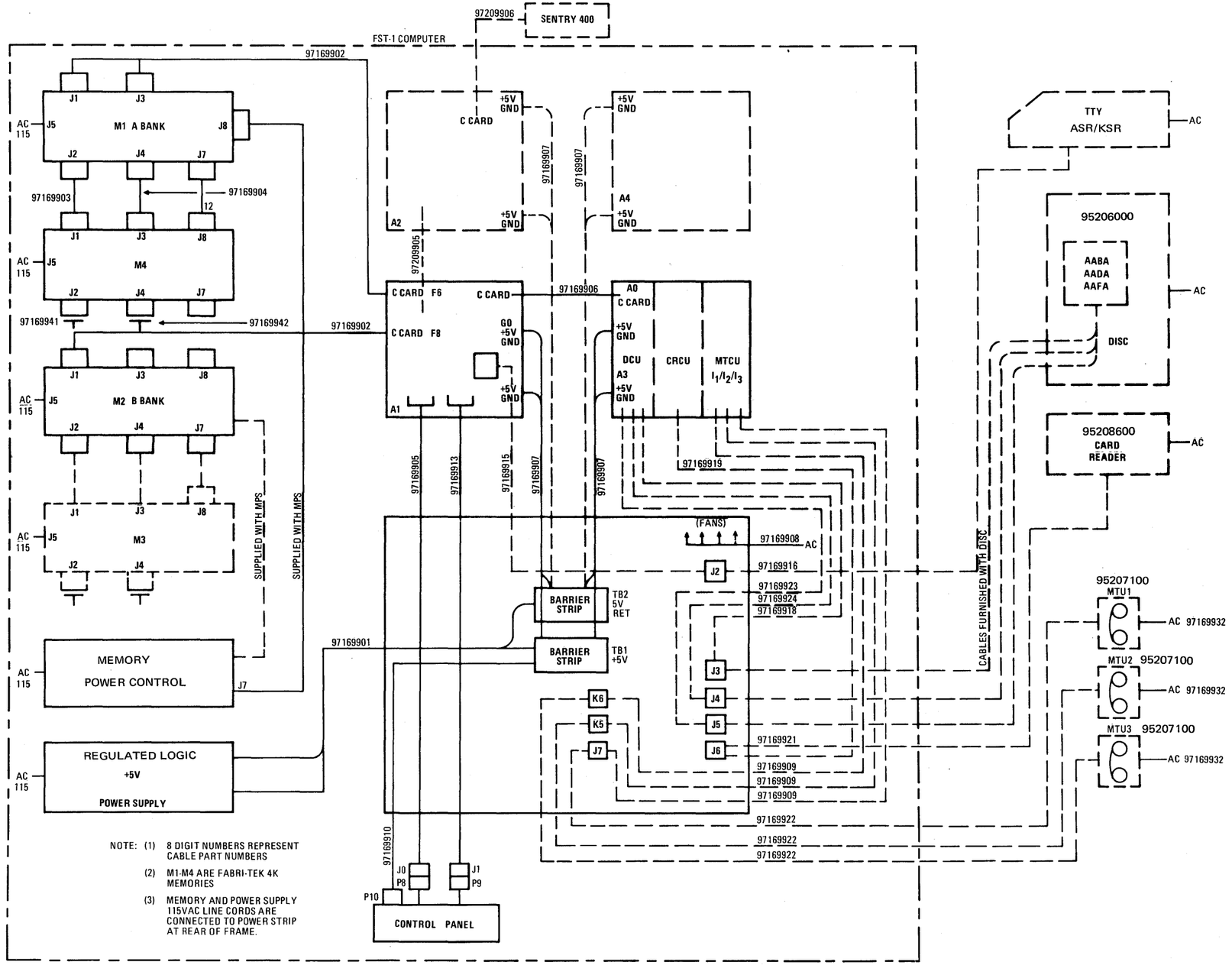

Figure 2-4. Interconnecting Cabling FST-1 Computer and Peripherals

Section III
Operation

3.1 INTRODUCTION

This section provides the operator with all necessary information to operate the Sentry 400 Test System in any testing environment, i.e., production testing, engineering development, or test engineering. Included is a description of the control and indicators for the FST-1 computer, test console, teletype and disc memory, as well as all optional peripherals available at this time. Also included are instructions for turning system power on and off, and loading CPU executive routines, utility routines, FACTOR, the Sentry 400 Tester OPerating SYstem Program (TOPSY), and device test programs.

3.2 CONTROLS AND INDICATORS

Keys and switches on the CPU Front Panel provide manual control of the FST-1 computer portion of the test system. The contents of various registers may be displayed visually on indicator lamps. The lamps light to denote the presence of a binary "1" in specific register bits as well as control and program switch flip-flops.

Switches and pushbuttons on the test station console allow the operator to manually control the mode of operation of the test system. In addition, the Front Panel indicators and displays inform the operator of test information such as DC and functional test pass or test fail, function test logical inputs and expected outputs, Go/No-Go results for each output pin during function testing, etc.

The Monitor Panel controls permit the operator to intervene, and manually vary the output voltages of various system reference power supplies. The reference supply outputs can also be monitored by a digital voltmeter. The MONITOR switch enables the Teletype key board for TOPSY command entries.

The ASR-33 Teletype is the primary input/output device for the system; optional input/output devices that can be redefined by the operator as the respective primary device include the Card Reader, Line Printer and Mag Tape.

The functions and location of the controls and indicators for the FST-1 Computer Test Console, Teletype, Disc Memory, Card Reader, and Line Printer are found in Tables 3-1 through 3-9 and Figures 3-1 through 3-10.

Table 3-1. FST-1 CPU Controls and Indicators

Panel Lock Switch	When in the counterclockwise position, this key-operated switch disables most CPU switches. (Switches not disabled are START, STOP, RESET, LOAD MT, LOAD CDR, and Console Sense Switches 1 through 6.) In the disable condition, inadvertent switch operation cannot disturb the program. The program can, however, read the contents of the switch register by execution of the RSR instruction.
START Pushbutton/ Indicator	Pressing this pushbutton switch illuminates the START indicator and causes the CPU to start executing program instructions, beginning with the instruction currently held in the command register. While the START indicator is lit, all CPU control switches are disabled except STOP, SIC, and SMC.
STOP Pushbutton/ Indicator	Pressing this pushbutton switch halts the program processing at the termination of the instruction currently being executed, turns off the START indicator, and turns on the STOP indicator. While the STOP indicator is lit, all console control switches are enabled if the SIC Switch is up.
SIC Switch	When in the up (ON) position, this switch halts the CPU at the end of the last memory cycle of the program instruction being executed: repeated depression of the START switch steps the program one instruction at a time. This switch is off in the down position.
SMC Switch	When in the up (ON) position, this switch halts the CPU at the end of one memory cycle-of-operation: repeated depression of the START switch steps the program one memory cycle at a time so the contents of the various register displays and indicators may be examined. This switch is off in the down position.
RESET Pushbutton	Pressing this switch resets the control flip-flop and initializes the program counter to 00100_8.
Switch Register Switches	These switches provide a means of manually setting up a 24-bit word, where a switch in the up position represents a binary "1" and down is a "0." The contents of the Switch Register are loaded into the program counter by the LDP switch, into the command register by the LDCR switch, into the A-register by the LDA switch, or by executing an RSR instruction.

Table 3-1. FST-1 CPU Controls and Indicators (Continued)

LOAD CDR Pushbutton	Pressing this switch causes the card reader to read a single card: the binary data on the card is loaded into 40 consecutive core memory locations beginning with address 00100_8. This switch is primarily used to read the first card of the six-card Card Object Loader (COL) program or the two-card Disc Bootstrap Program.
LOAD MT Pushbutton	Pressing this pushbutton switch causes the Magnetic Tape DOPSY System Bootstrap program to be read from magnetic tape and to be stored into 40 consecutive core-memory locations beginning with address 00100_8. With the Magnetic Tape DOPSY System Bootstrap Program resident in core memory, program control is transferred to the DOPSY monitor, by loading the instruction BRU 100 (01000100_8) into the command register and then pressing the START pushbutton.
LDA Switch	Lifting this spring-loaded switch causes the contents of the switch register to be loaded into the A-register. SIC must be on to enable this function.
LDP Switch	Lifting this spring-loaded switch loads the contents of the switch register into the program counter. SIC must be on to enable this function.
LDC Switch	Lifting this spring-loaded switch loads the contents of the switch register into the command register. SIC must be on to enable this function.
CLK Switch	The clock two-position switch is off in the down position. When in the up (ON) position, it prevents the content of the command register from being changed after the instruction in that register has been executed; it also causes the contents of program counter bits 0 thru 11 and command register bits 12 and 13 to be used as the effective operand address instead of the actual operand address specified by the instruction in the command register. Each time the instruction is executed the content of the program counter is incremented by one, thereby modifying the effective operand address. This switch, when used with the SIC and START switches, affords an alternate means to load manually or to examine consecutive core-memory locations, one at a time, with either the STA or LDA instruction, respectively, in the command register. It may be used also to clear core memory by loading a STA instruction in the command register, zero in the A-register, and then pressing START.

Table 3-1. FST-1 CPU Controls and Indicators (Continued)

STW Switch	Lifting this spring-loaded switch stores the contents of the switch register in the buffer register and the core-memory location specified by the current content of the program counter. When the store operation is completed, the program counter is then incremented by one. Thus, information in sequential memory addresses may be stored by repeated operation of the STW switch.
EXM Switch	Lifting this spring-loaded switch loads the contents of the core-memory location specified by the current contents of the program counter into the buffer register for visual examination by the operator. When the examine operation is completed, the program counter is incremented by one. Thus, the contents of sequential core memory addresses may be examined by repeated depression of the EXM switch.
P COUNT Indicators	Indicates the content of the 14-bit program counter. In the STOP state, the program counter holds the core memory address of the next instruction word that will be loaded into the command register, if the current instruction is not a branch instruction.
Register Display Indicators	Indicates the contents of the 24-bit register selected by the appropriate register-display-select pushbuttons.
Register-Display-Select Pushbuttons	Each of the 12 pushbuttons, when pressed, cancels the previously pressed pushbutton and causes the contents of its associated register to be displayed by the register-display indicators. The function of each of the selectable register displays is as follows:
A-Register Display	Indicates the content of the 24-bit accumulator register. The accumulator is the main arithmetic register for such operations as ADD, SUB, MUL, and DIV occur, as well as the logical operations of AND and OR. It also serves as the input/output register for the transfer of data under program control.
E-Register Display	Indicates the content of the 24-bit extension register. This register is an extension of the accumulator register and is used with double-precision arithmetic instructions such as DADD, DSUB, MUL, and DIV.
C Register Display	Indicates the content of the 24-bit command register. In the idle state, the command register stores the next instruction word.

Table 3-1. FST-1 CPU Controls and Indicators (Continued)

B-Register Display	Indicates the content of the 24-bit buffer register. All information written into or read out of core memory from the CPU during the execute phase is temporarily held in the buffer register. This information can thus be monitored by the operator using the STW and EXM switches while the SIC (single instruction cycle) or the SMC (single memory cycle) switch is on.
X_0 thru X_7 Register Display	Indicates the contents of the selected 14-bit index register.
Console Sense Switches	The six console sense switches manually control the execution sequence of any program that contains appropriate BOS instructions. A switch in the up position represents a binary "1," and down represents a binary "0." The state of each switch may be individually tested with a BOS instruction.
Program-Sense-Switch Indicators	Each of the eight lamps indicates the state of its corresponding program-sense-switch flip-flop. The state of a program-sense-switch flip-flop may be used to automatically control the execution sequence of any program that contains appropriate BOS instructions. An illuminated lamp indicates its corresponding program-sense-switch flip-flop has been set to the "1" state by a SST instruction. Each flip-flop can be reset to the "0" state, turning its lamp off, with a RST instruction. The state of each program-sense-switch flip-flop may be individually tested with a BOS instruction.
Peripheral-Status Indicators	Each of the nine lamps, when lit, indicates a particular status condition of its associated peripheral device. The definition of each indicator mnemonic follows:

Mnemonic	Definition
PEA	Memory "A" parity error
PEB	Memory "B" parity error
MBA	"A" memory is busy
MBB	"B" memory is busy
DER	Disc parity error
DBU	Disc is busy
MER	Magnetic tape error
MTB	Magnetic tape is busy
INP	Input pending

PEA	This indicator will be illuminated when an "A" memory parity error is detected, if the system is equipped with that option.
PEB	Performs same function for "B" memory as PEA indicator.

Table 3-1. FST-1 CPU Controls and Indicators (Continued)

MBA	When illuminated, indicates that the "A" memory is being accessed.
MBB	Performs same function for "B" memory as "A" indicator.
DER	When illuminated, indicates that a disc parity-check error has been detected.
DBU	The disc busy flip-flop is set, lighting the DBU indicator, when the disc is performing an operation such as read, write, or parity check. The flip-flop is reset, turning the indicator off, when the operation is completed.
MER	Magnetic tape parity error
MTB	Magnetic tape is busy.
INP	The input-pending flip-flop is set, lighting the INP indicator, by an ION instruction. This indicator is a visual indication only to the operator that the program is expecting data from an input device. The flip-flop is reset, turning the indicator off, by an IOFF instruction or by depressing the RESET switch. The state of the flip-flop cannot be tested; hence, it cannot control the program-execution sequence.

Status Register Flip-Flop Indicators

Each of the six lamps indicates the state of its associated status-register flip-flop. The mnemonic definition of each indicator follows:

Mnemonic	Definition
GT	Greater than
EQ	Equal
LT	Less than
BE	Bit equal
OV	Overflow
SN	Sign

The indicators GT, EQ, LT, BE, and OV are lighted (with the associated flip-flop set) in various configurations after executing one of the instructions CAM, ATX, SPU, or BRU* (BRU with indirect bit set). The indicators affected by each instruction are shown below; refer to the detailed description of each instruction to interpret the meaning of each indicator for that specific condition.

Table 3-1. FST-1 CPU Controls and Indicators (Continued)

	Instruction **Used** CAM GT, EQ, LT, BE ATX GT, EQ, LT, (ignore BE state) SPU GT, EQ, LT, BE BRU* GT, EQ, LT, BE, OV.
OV Indicator	The overflow flip-flop will be set and the OV indicator lighted, in addition to a BRU* instruction, by one of the following conditions: If the accumulator overflows as the result of executing an ADD, SUB, DADD, DSUB, or DTC instruction; by executing the appropriate SST instruction. The overflow flip-flop can be reset, turning off the OV indicator by executing the appropriate RST instruction.
SN Indicator	The SN indicator indicates the sign of the number left in the accumulator. Under these conditions, the SN indicator is interpreted as follows: **Condition** **Interpretation** OFF Number in AC is positive ON Number in AC is negative
Control Flip-Flop Indicator	Each of the four lamps indicates the state of the corresponding control flip-flop. The definitions of indicator mnemonics follow: **Mnemonic** **Definition** IER Instruction Error IEN Interrupt Enable TIF Time of Instruction Fetch TOF Time of Operand Fetch
IER	The IER (Instruction Error) flip-flop is set, illuminating the IER indicator, as the command register is loaded, either from core memory or the switch register, with an instruction containing an op code between 41_8 and 77_8, inclusive.
IEN	The interrupt-enable flip-flop is set and the IEN indicator lighted as the result of executing an IEN instruction. The flip-flop may be reset, turning off the indicator, by executing an IDA instruction, by executing a priority interrupt, or by pressing the RESET pushbutton.
TIF	When executing any instruction, the TIF (time-of-instruction-fetch) flip-flop will be set, illuminating the TIF indicator, while the CPU is in the instruction-fetch cycle.

Table 3-1. FST-1 CPU Controls and Indicators (Continued)

	During the instruction-fetch cycle, the contents of the program counter are transferred to core memory and decoded. At the T1 phase of the instruction-fetch cycle, the contents of the decoded memory address are gated into the command register, and the program counter is incremented by one in readiness for the next instruction-fetch cycle; the TIF flip-flop is reset at the end of this T1 phase.
TOF	When executing any memory-reference instruction, the TOF (time-of-operand-fetch) flip-flop is set, illuminating the TOF indicator, while the CPU is in the operand-fetch cycle. During the T1 phase of an operand-fetch cycle, the contents of the instruction operand are gated into the buffer register. If the instruction requires only one operand, the TOF flip-flop is reset at the end of the T1 phase of the operand-fetch cycle. If two operands are required, TOF is reset at the end of the second operand-fetch cycle.

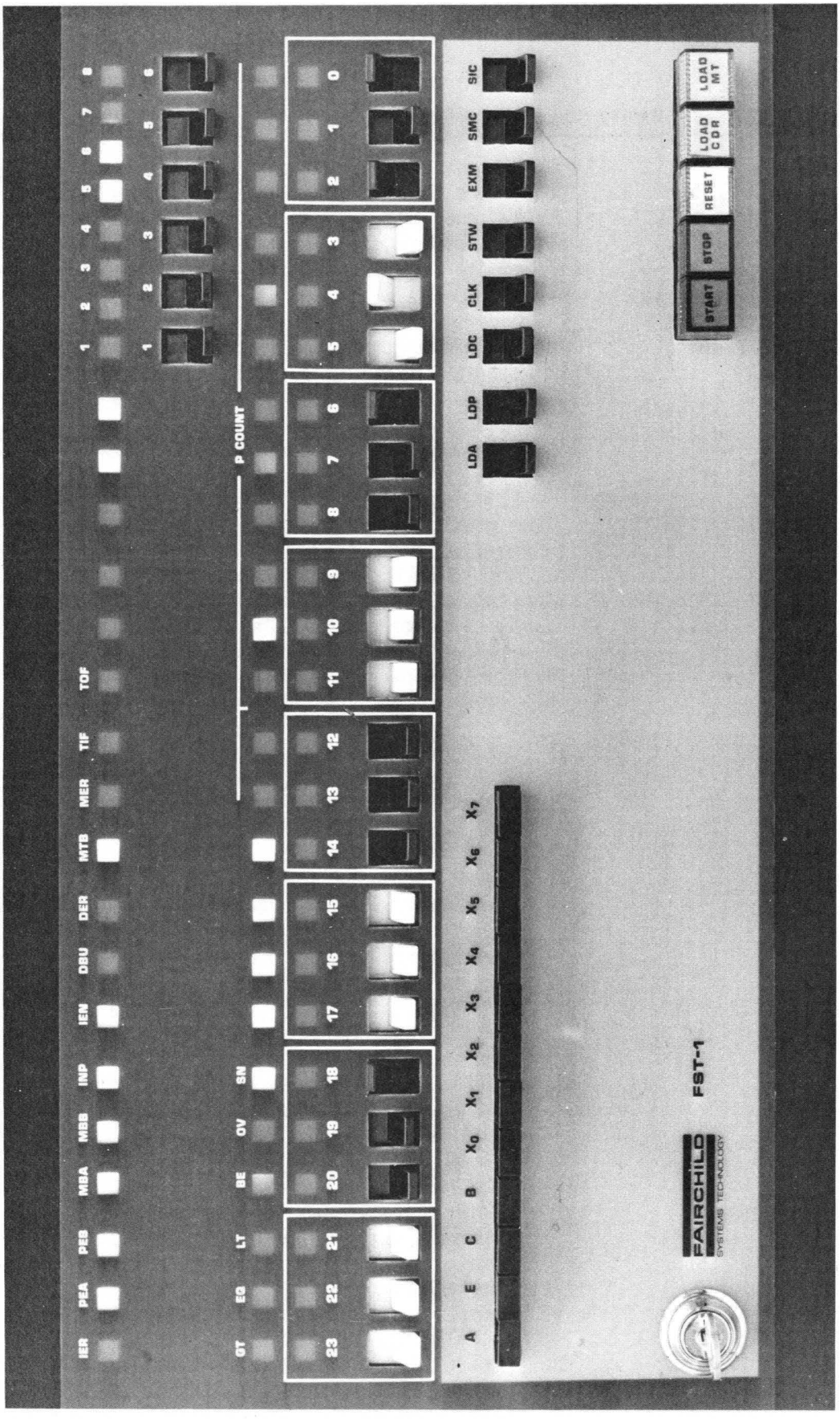

Figure 3-1. FST-1 Computer Control Panel

Table 3-2. Sentry 400 Test Station Console, Controls and Indicators

POWER Key	Turning this key in the clockwise direction applies primary AC power to the test console, DC power supplies, fans, DVM's and core memories. Primary AC power is also supplies to the system input/output peripherals but is controlled by "power on" switches or pushbuttons on the respective units.
POWER RESET Pushbutton	Depressing this pushbutton applies power to the test station console after the Power key has been rotated clockwise. The mainframe power must be on before power can be enabled at the station.
POWER FAIL Indicator	Cycles on and off when a power failure occurs.
REGISTER SELECTOR Pushbuttons	These pushbuttons allow the operator to select two "Long Registers" whose contents will be simultaneously displayed by the REGISTER DISPLAY LAMPS. Each pushbutton when pressed cancels the previously pressed pushbutton and causes the contents of the associated register to be displayed. In the following description of each "Long Register" a binary "1" is represented by a lighted lamp while an unlighted lamp represents a binary "0": F: Function Register—represents the input forcing logic for those pins programmed as "Inputs" and the expected output response for those pins programmed as "Outputs" in the D Register. M: Mask Register—controls the "care" or "don't care" condition for each tester pin. A binary "0" or "don't care" inhibits the comparison operation for that particular pin, while a binary "1" or "care" enables the comparison operations. R: Utility Relay Register—controls the utility relays, one per tester pin. A binary "1" indicates a closed relay and a binary "0" indicates an open relay. The utility relays can be used for such functions as to connect a load resistor for an output pin to a programmable power supply. S: Select Reference Register—selects which set of reference supplies are to be used by the functional test driver for each tester pin. A binary "0" selects the E0/E1 reference supplies while a binary "1" selects the EA0/EA1 reference supplies. D: Input/Output Pin Definition Register—this register defines each tester pin as an input pin or an output pin. A binary "1" represents an input and a binary "0" represents an output for its associated tester pin.

Table 3-2. Sentry 400 Test Station Console, Controls and Indicators (Continued)

	C: Comparison Register—this register stores the Go/No-Go results of a comparison between the actual outputs of a device and the expected outputs. A binary "1" represents a comparison failure and a binary "0" represents a pass condition.
Register Display Indicators	This display, consisting of two horizontal rows of lamps numbered from 1 to 15, allows the operator to simultaneously examine the contents of one rank of two selected Long Registers. The bottom row, or row 2, can display the contents of the F, M, or R Register; the top row, or row 1, can display the contents of the S, D, or C Register.
RANK SELECTOR Pushbuttons	There are 8 ranks to each register. The register to be displayed is selected by the REGISTER SELECTOR and the rank of pins to be displayed, is selected by the RANK SELECTOR. Since there are 8 ranks for each register, the status of all 120 pins (8 x 15) can be displayed by the appropriate combination of REGISTER SELECTOR and RANK SELECTOR. e.g., if it is necessary to display the status of all 120 pins of the "S" register, the REGISTER SELECTOR "S" button is depressed. Each rank of 15 pins may now be displayed by depressing in turn RANK SELECTOR buttons 1 thru 8.
RANK FAIL INDICATOR	If a functional failure occurs at a pin, the RANK FAIL INDICATOR associated with the rank of pins to which the failed pin belongs, will illuminate. To determine the failed pin, the failed rank of pins may be selected by the RANK SELECTOR and displayed on the Register Display Indicators.
STATEMENT NUMBER Display	This is a five-digit octal display of the test instruction number from 00000_8 to 77777_8. Each time a tester statement or instruction is executed the statement number display is incremented by one. This display will read 00001 while an automatic test is in progress and be updated with the last test number at pauses.
EXTERNAL REGISTER Display	Provides a display of the ten least significant bits of the external interface register.
LAMP TEST Pushbutton	This pushbutton, when depressed, will cause all display panel lights to light, if they and their associated drivers are operational.
START Pushbutton/Indicator	This pushbutton, when depressed, produces a START pulse that initiates active testing of the device-under-test.

Table 3-2. Sentry 400 Test Station Console, Controls and Indicators (Continued)

MANUAL Pushbutton/Indicator	When ON, one tester statement or instruction is executed each time the START switch is depressed until all statements have been executed. NOTE: If the MAN switch is not depressed and the system is not in MONITOR, the system is in automatic mode.
ADV Pushbutton/Indicator	While depressed, and in the MANUAL test mode, this momentary switch allows START pulses to be generated at a repetition rate of three per second. This allows the operator to perform such operations as verification of the test program currently stored in core memory; this feature also allows the operator to advance the test program to a specific function test number of interest for the purpose of varying the programmed voltage parameters normally applied to the device during that test while observing the results. The START button should be depressed once before using ADV.
ON LINE Indicator	Indicates that particular station is on line to the system.
RESET Pushbutton/Indicator	This momentary switch, when depressed, resets all tester displays and registers with the exception of the STOP ENABLE bit in the Status (STAT) Register. This operation also sets the STOP bit in the STAT Register.
FUNCTION TEST PASS/FAIL Indicators	At the completion of a function test the appropriate indicator will light to signify the PASS or FAIL status of the device for that test, or sequence.
PARAMETER TEST PASS/FAIL Indicators	At the completion of a DC parameter test, the appropriate indicator will light to signify the PASS or FAIL status of the device for that test, or sequence.
EOT Indicator	The EOT indicator (End-of-Test) is illuminated after the last statement of a test program has been executed.
EXTERNAL SYNC	Under program control a SYNC pulse will be available at this jack. The pulse may be used to trigger an oscilloscope or some other equipment defined by the user.
GROUND	System ground.

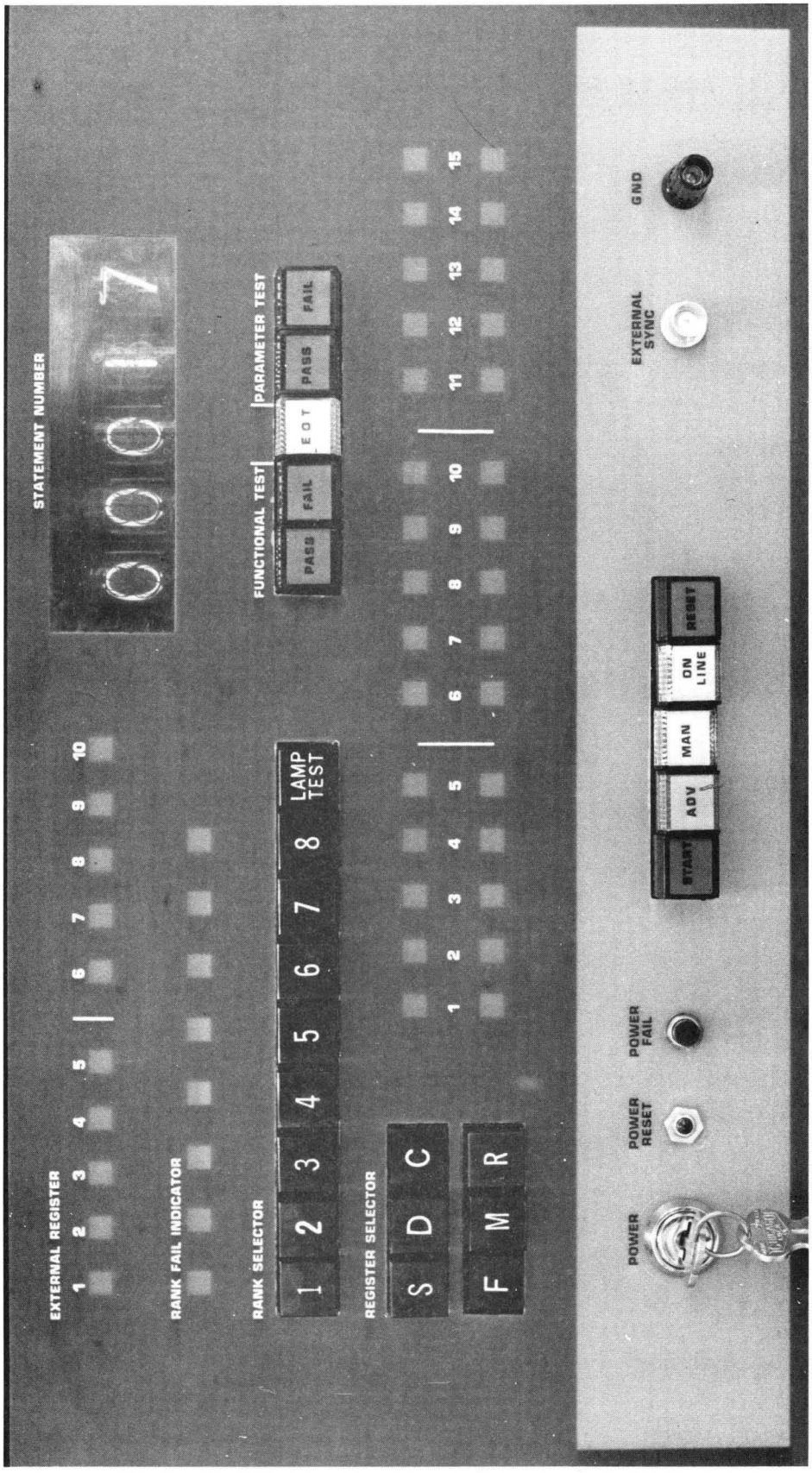

Figure 3-2. Sentry 400 Test Station Console Control Panel

Table 3-3. Sentry 400 Monitor Control Panel Controls and Indicators

POWER/OFF/ON Key	Turning this key to the ON position and pressing the RESET button will apply primary power to the system. All electronics in the main frame will power up at this time. Individual peripheral devices, test stations, ~~and memories~~ must be turned on via their individual power on switches.
RESET Pushbutton	When the POWER OFF/ON key is set to the ON position, pressing this pushbutton applies power to the system as described above.
MUX INHIBIT OFF/ON Key	Rotating this key switch clockwise gives complete control to station No. 1. Stations No.'s 2, 3, and 4 are inhibited from operation.
PROGRAM Indicator	The program indicator indicates that all DPS's and RVS's are under program control.
MANUAL Indicators	When illuminated indicates that one or more of the DPS's or RVS's is being manually overridden.
POWER Indicator	When illuminated indicates primary power is on for the main frame. If one of the supplies fail,the indicator will flash and an audible alarm will be heard.
MANUAL ADJUST POWER SUPPLY Pushbuttons STATIONS-1 -2 -3 -4 RELEASE	Depressing any one of these buttons permits the station selected to manually adjust the DPS's and RVS's via the manual controls, if that station is on line. Depressing the RELEASE pushbutton returns the selected station to program control. Only one station at a time may be selected for manual operation.
HI LO GUARD Jacks	Allows the user to connect any external voltage for display on the DVM, when the EXT pushbutton is depressed.
MON Pushbutton/Indicator	When TOPSY is resident in core memory and the MON pushbutton is depressed, the user can enter TOPSY commands via the primary input device (usually TTY). The TTY is disabled for datalogging.
STROBE Pushbutton/Indicator	When the STROBE pushbutton is depressed and the test station is in the MANUAL mode of operation, the function test comparators will be repetitively strobed at approximately 1.5MHz. This allows the user to vary programmed DPS or RVS voltages to assist in determining device pass/fail threshold values.

Table 3-3. Sentry 400 Monitor Control Panel Controls and Indicators (Continued)

SYNC Pushbutton/Indicator	When the SYNC pushbutton is depressed and the system is in MANUAL mode of operation, SYNC signals will occur repetitively at a rate con trolled by the TD (Time Delay) register.
Digital Voltmeter Display	The Nixie light display provides a five-digit plus sign display of all monitored voltages. If the AUTO RANGE button is depressed, automatic ranging of the decimal point occurs. If the REMOTE pushbutton is selected the decimal point is located according to the 1, 10, 100, 1000, 10000, range selector pushbuttons. The DVM can also measure resistance at the external jacks with the kilolm button and EXT depressed.
EXT Pushbutton	Depressing this pushbutton will permit any voltage connected to the HI LO GUARD terminals to be displayed on the DVM.
PMU Pushbutton	Depressing this pushbutton will permit any voltage being monitored by the precision measurement unit (PMU) to be displayed on the DVM.
DPT1, DPT2, DPT3	Depressing the appropriate pushbutton will display a voltage proportional to the current the DPS1, DPS2 or DPS3 are supplying. Scale factors are 100 microamps per millivolt if the DPS is in the 100mA current range and 1 milliamp per millivolt on the 1 ampere range.
DPS1 Pushbutton	Depressing this pushbutton permits the programmed DPS1 supply voltage to be displayed on the DVM. If the DPS1 polarity switch (+ OFF -) is set to the + or - position, the DVM will display the manually adjusted DPS1 supply voltage.
DPS1 Fine Adjustment Coarse Adjustment + OFF – (polarity switch)	The DPS1 coarse and fine adjustments permit manual variation of the DPS1 supply voltage, (Manual over-ride of programmed voltage), when the polarity switch (+ OFF -) is set to + or -. A three digit counter connected to the COARSE ADJUST knob displays the approximate value of the voltage selected by the coarse adjustment control. The coarse adjustment may be varied to a maximum 9.99 volts as displayed on the digital counter. If a back lighted 10V x 4 appears directly above the three digit counter, the three digit readout must be multiplied by 4 to obtain the true output value. The manually adjusted voltage may be displayed on the DVM by depressing the DPS1 pushbutton.
DPS2, DPS3, S0, S1, E0, E1 EA0, EA1, EB0, EB1, EC0, EC1	Same functions and operation as DPS1.

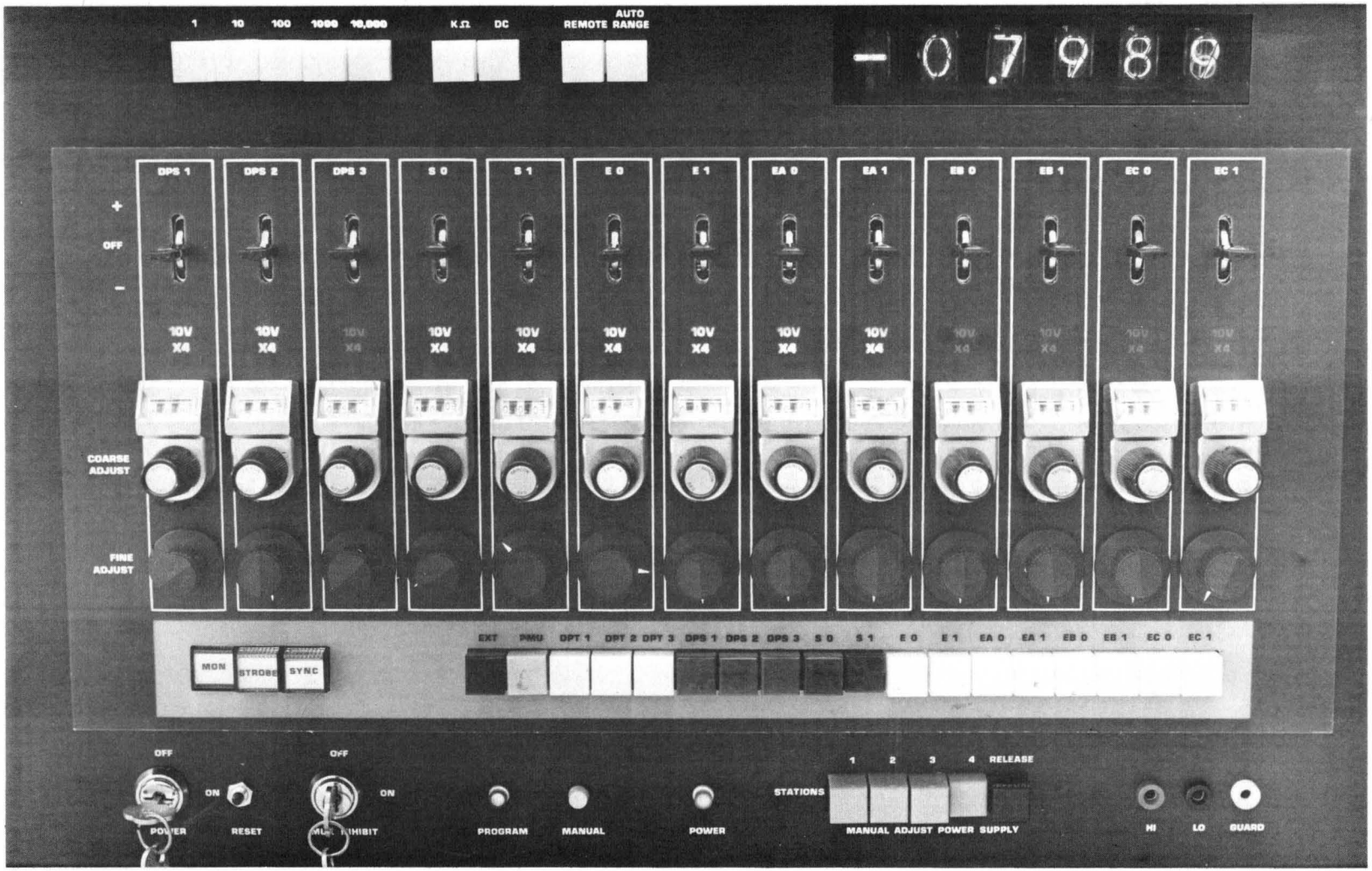

Figure 3-3. Sentry 400 Monitor Station Control Panel

Table 3-4. FST-1 2084 Teletype Model ASR-33 Controls and Indicators

Unit	Control	Description
Teletype	LINE/OFF/LOCAL Switch	Controls application of primary power in the Teletype and controls data connection to the CPU. In the LINE position the Teletype is energized and connected as an I/O device of the computer. In the OFF position the Teletype is de-energized, i.e., primary power is removed. In the LOCAL position the Teletype is energized for off-line operation, and signal connections to the CPU are broken.
Paper Tape Punch	REL Pushbutton	Disengages the tape in the punch to allow tape removal or tape loading.
	B. SP. Pushbutton	Backspaces the tape in the punch by one space, allowing manual correction or rub out of the character just punched.
	ON Pushbutton	Turns TAPE PUNCH on for simultaneous operation with Teletype keyboard/printer.
	OFF Pushbutton	Turns TAPE PUNCH off.
	START/STOP/FREE Switch	Controls use of the tape reader with operation of the Teletype. In the lower FREE position the reader is disengaged and can be loaded or unloaded. In the center STOP position the reader mechanism is engaged but de-energized. In the upper START position the reader is engaged and operated under program control.
Keyboard		Provides a means of printing on paper when used as a typewriter and punching tape when the punch ON pushbutton is depressed; also provides a means of supplying input data to the computer when the LINE/OFF/LOCAL switch is in the LINE position.

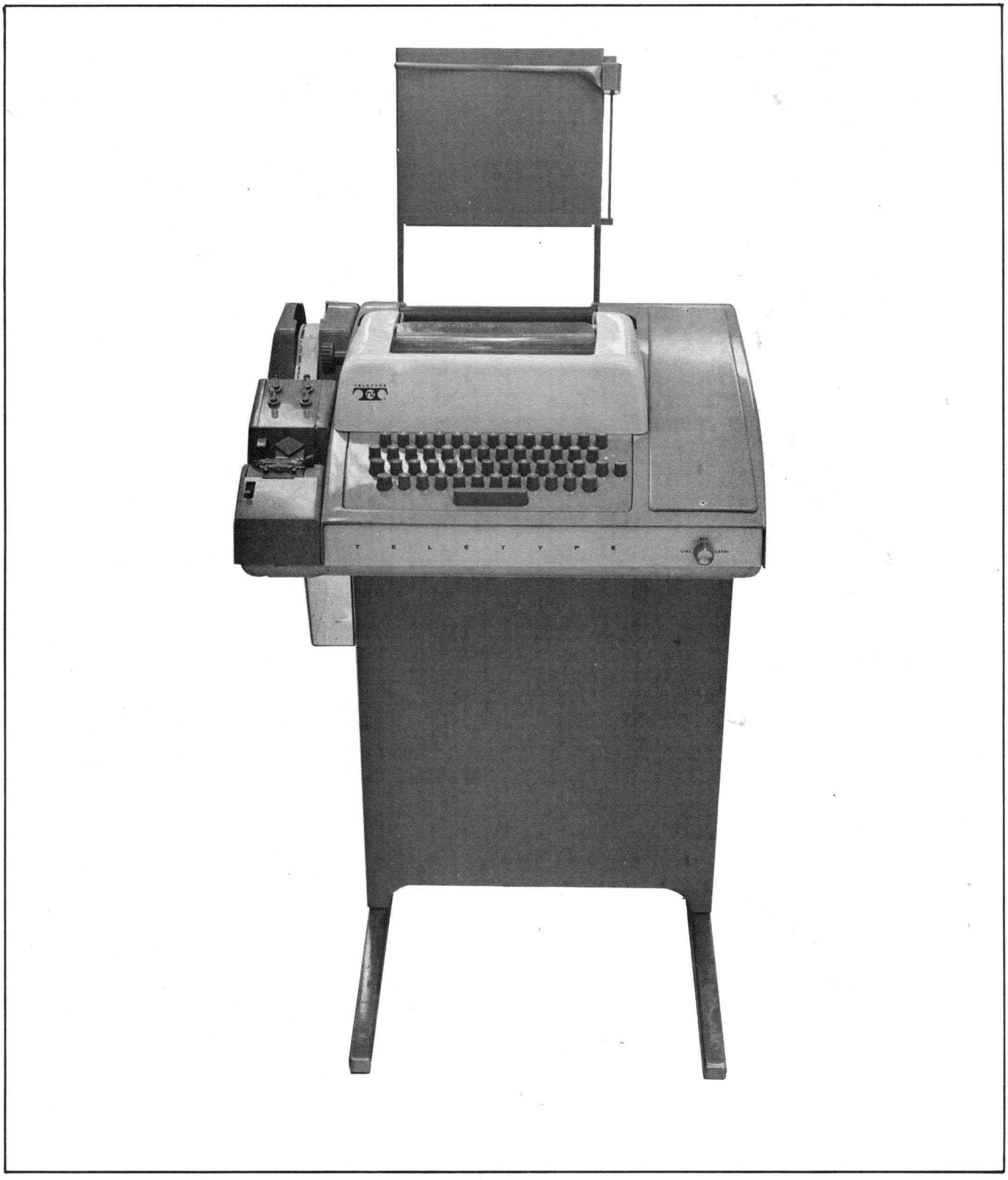

Figure 3-4. Teletype Model ASR-33

Table 3-5. FST-1 2085 Teletype Model ASR-35 Controls and Indicators

Unit	Control	Description
Teletype	LINE/OFF/LOCAL Switch	Controls application of primary power in the Teletype and controls data connection to the CPU. In the LINE position the Teletype is energized and connected as an I/O device of the computer. In the OFF position the Teletype is de-energized, i.e., primary power is removed. In the LOCAL position the Teletype is energized for off-line operation, and signal connections to the CPU are broken.
	Break Pushbutton/ Indicator	This pushbutton/indicator is illuminated if keyboard or tape reader transmission is broken, either by internal means (refer to Teletype manual for theory of operation) or by pressing the pushbutton. Transmission can be restored by pressing the BRK RLS key on the keyboard.
	Rotary Mode Switch	This 5-position rotary switch, located to the left of the Teletype keyboard, is used to select the mode of operation when in LOCAL or ON LINE. The positions are as follows: K — keyboard KT — keyboard tape T — tape TTS — tape-tape send TTR — tape-tape receive Of the five, only the K, KT, and T positions are used when the ASR-35 is used with the Sentry 400 Test System. These positions are defined as follows: K All information, received or typed will be printed. KT A printed copy and punched tape will be produced of any information received or typed. T In the LOCAL or ON LINE mode, a punched tape only will be produced when using the keyboard. In the ON LINE mode, a printed copy will be produced of any information received from the system.

Table 3-5. FST-1 2085 Teletype Model ASR-35 Controls and Indicator (Con't)

Unit	Control	Description
Paper Tape Reader	START/STOP/FREE Switch	Controls use of the tape reader with operation of the Teletype. In the lower FREE position the reader is disengaged and can be loaded or unloaded. In the center STOP position the reader mechanism is engaged but de-energized. In the upper START position the reader is engaged and operated under program control.
Keyboard		Provides a means of printing on paper when used as a typewriter and punching tape when the punch is on; also provides a means to supply input data to the computer when the LINE/OFF/LOCAL switch is in the LINE position. A number of supplementary keys are present which provide the following functions: BRK RLS — Turns off BREAK light and restores keyboard/tape reader transmission. LOC LF — Causes the paper to feed out of the printer at an accelerated rate. LOC CR — Releases the type box carriage allowing it to return to the left. LOC BSP — Backspaces the tape punch one space each time the key is depressed. REPT — If simultaneously depressed with any character key, the character will be continuously repeated until the REPT key is released.

Figure 3-5. Teletype Model ASR-35

Table 3-6. FST-1 Model 2060 Disc File Controls and Indicators

Control/Indicator	Description
POWER ON Pushbutton/ Indicator	Depressing this pushbutton applies primary AC power to the disc memory and illuminates the POWER ON pushbutton; also illuminates the NOT READY indicator.
POWER OFF Pushbutton	Depressing this pushbutton removes primary AC power from the disc memory, turning off the NOT READY indicator and POWER ON pushbutton illumination.
NOT READY Indicator	This indicator is illuminated when any of the following System Ready conditions are not met: 1. Power On. (A.C. and D.C. power supplies) 2. Disc up to speed 3. Adequate reserve pressure in the air supply system. 4. Heads flying, 5. Touch circuit in Fly Ready Status.

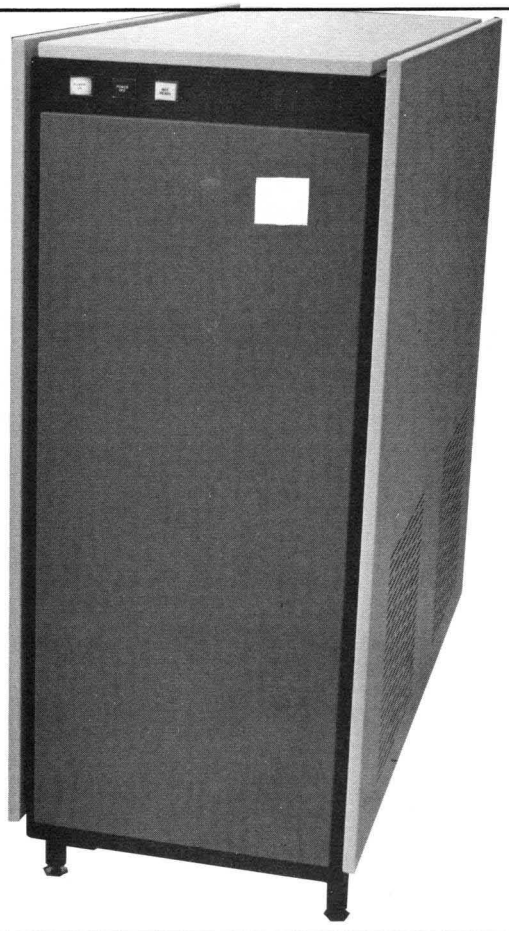

Figure 3-6. FST-1 Model 2060 Disc Memory

Table 3-7. FST-1 Model 2086 Punched Card Reader Controls and Indicators

STOP White Pushbutton/ Indicator	This momentary action pushbutton/indicator stops operation and places the unit in a standby mode of operation when pressed.
START Yellow Pushbutton/ Indicator	This momentary action pushbutton/indicator, starts the unit motor and drive train. It also clears and resets the logic when pressed.
HOPPER Amber Indicator	When this indicator lights, the input hopper is empty or the output stacker is full.
READY Amber Indicator	When lighted, on-line operation of the unit can begin or resume. An error condition or failure to feed a card will cause this light to go out.
FEED Amber Indicator	When lighted, a feed irregularity, a nonfeed, or interlock switch open condition is present. After the malfunction is cleared, the START pushbutton must be pressed to restart operation of the unit.
READ Amber Indicator	When lighted, indicates that a card has failed to read properly.
OFF Red Pushbutton/ Indicator	This momentary action pushbutton when pressed, cuts off AC power to the unit.
ON Green Pushbutton/ Indicator	This momentary action pushbutton/indicator when pressed, applies AC power to the power supply and logic circuits. This indicator is lighted green when power is on.

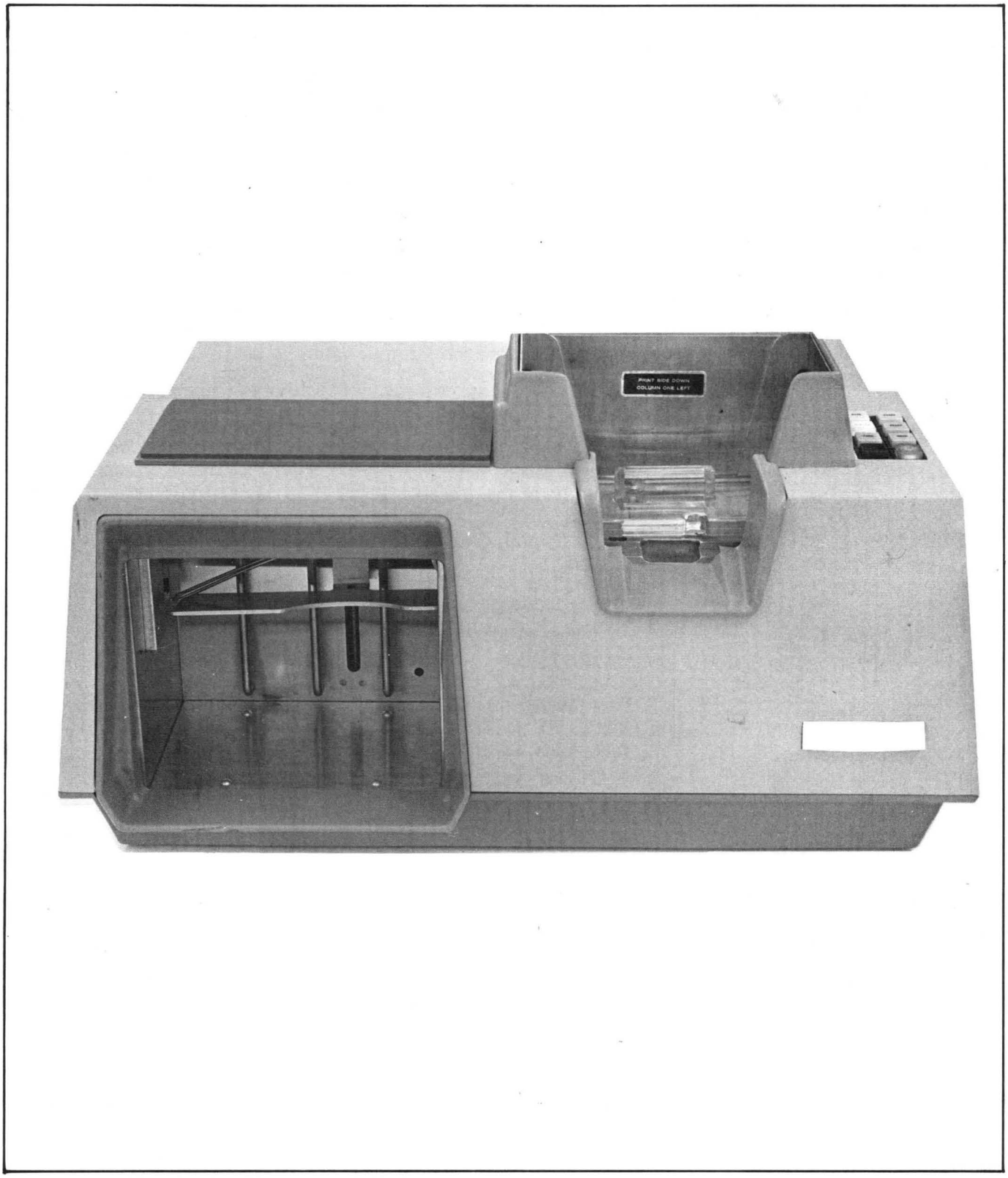

Figure 3-7. FST-1 Model 2086 Punched Card Reader

Table 3-8. Model 2071 Magnetic Tape Unit Controls and Indicator

Control/Indicator	Description
HIGH/LOW DENSITY Switch (Slides)	Controls delay of read strobe pulse during reading. This must be set to high density, 800 BPI.
REVERSE - Momentary ON pushbutton	Initiates movement of tape in reverse direction at normal operating speeds.
REWIND - Momentary ON pushbutton	Initiates movement of tape in reverse direction at high speed until BOT marker is reached.
STOP-RESET - Momentary ON pushbutton indicator	Stops all tape movement, resets control circuits and returns transport from remote to local control. Switch indicator illuminates in local mode.
FORWARD - Momentary ON pushbutton	Initiates movement of tape in forward direction at normal operating speed. Forward tape motion stops when tape reaches EOT tab.
FAST-FORWARD - Momentary ON pushbutton	Initiates movement of tape in forward direction at high speed. Forward tape motion stops when tape reaches EOT tab. The tape unit will not detect a BOT marker.
REMOTE - Momentary ON pushbutton	Sets transport to remote. On-line control switch indicator illuminates in Remote mode.
POWER - indicator lamp	Illuminates when regulated +12 vdc current is available at transport.
FILE PROTECT Indicator lamp	Illuminates when write enable ring is not in place, indicating that tape data is protected. Also illuminates when no reel is installed on file reel.
INTERLOCK - Automatic door operated switch	Prevents tape movement, read or write operation, and tape spillage when door is open during operation. Storage arms retract to local position, and reels take up resultant tape slack. When switch is pulled outward, permits operation with door open.
BRAKE RELEASE SWITCH - Momentary Button	This switch releases the reel brakes to facilitate loading of tape.

All controls and indicators, except the HIGH/LOW DENSITY, INTERLOCK and BRAKE RELEASE switches are located on the operator control panel. All other switches are located at the bottom of the INTERNAL front panel.

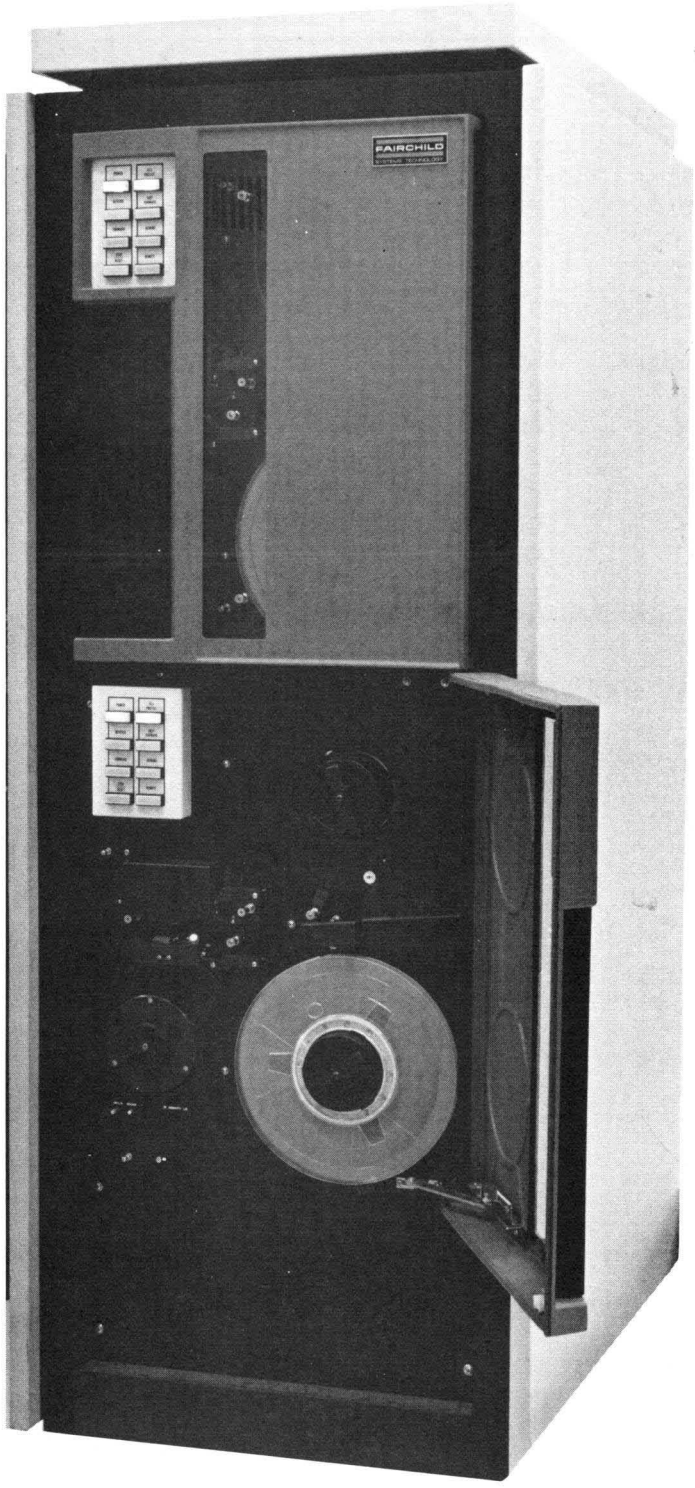

Figure 3-8. Model 2071 Magnetic Tape Unit

Table 3-9. FST-1 Model 2310 Line Printer Controls and Indicators

Control Panel

Control/Indicator	Description
POWER Indicator	Lights when AC power is applied to line printer.
READY Indicator	Lights when printer power is on, interlocks are satisfied, and PRINT INHIBIT switch is off.
ON LINE Indicator	Lights when printer is in ON LINE mode of operation and PRINT INHIBIT switch is off.
ON LINE/OFF LINE Switch	Selects mode of operation for printer.
TOP OF FORM Switch	Advances tractors to top-of-form position. Disabled when in ON LINE mode.

Maintenance Panel

Control/Indicator	Description
DRUM GATE Indicator	Lights when drum gate is unlatched.
PAPER FAULT Indicator	Lights when paper is torn or missing.
PRINT INHIBIT Indicator	Lights when PRINT INHIBIT switch is in ON position.
PRINT INHIBIT Switch	Inhibits hammer drivers during maintenance.
MASTER CLEAR Switch	Initializes the printer to ensure that the logic elements are in proper states.
Main Power Circuit Breaker	Applies AC power to printer.

Figure 3-9. Model 2310 Line Printer Controls and Indicators

3.3 SYSTEM POWER ON PROCEDURE

The following procedure is used to apply power to the Sentry 400 Test System.

1. Set WRITE INHIBIT switch in the disc to the up position. ← This is not described in disc section pg 3-22
2. Set the MAIN POWER circuit breakers to the ON position.
3. Press POWER ON pushbutton on the disc memory unit. The POWER ON pushbutton and NOT READY indicator will illuminate. Wait for NOT READY lamp to extinguish. NOTE: It is recommended that the disc be left on at all times if possible to insure reliable operation.
4. Set SIC (Single Instruction Cycle) and SMC (Single Memory Cycle) on the FST-1 computer to the on (UP) position.
5. Turn the main frame Power key switch clockwise to the ON position then depress the RESET button.
6. Turn the Teletype LINE/OFF/LOCAL switch to the LINE position.
7. Turn the test station Power key switch clockwise to the ON position then depress the POWER RESET button.
8. Turn all other desired peripheral devices on by depressing the appropriate POWER ON pushbuttons.
9. Set WRITE INHIBIT switch to the down position in the DISC.
10. Load the DOPSY monitor (Sect. 3.5.1).

3.3.1 Power Failures and Alarms

If the AC power input fails for a period of more than 8 milliseconds, system power will be automatically turned off. To return system power, repeat power turn on procedure.

If a power failure occurs at the mainframe the power failure lamp at the mainframe will cycle on and off, also an audible alarm at the mainframe will be heard. If a power supply failure occurs in the test station, power failure lamps will cycle on and off, and audible alarms will be heard at the mainframe and affected stations.

3.4 SYSTEM POWER OFF PROCEDURE

The following procedure is used to remove power from the Sentry 400 Test System.

1. Set WRITE INHIBIT switch in the disc to the up position.
2. Set SIC and SMC switches on the FST-1 computer to the on (up) position.
3. Turn the test station key switch counter clockwise.

4. Set Teletype LINE/OFF/LOCAL switch to the OFF position.

5. Turn the mainframe key switch counter clockwise.

6. Press the POWER OFF pushbutton on the disc memory unit. NOTE: LEAVE DISC POWER ON EXCEPT FOR EMERGENCY.

7. Remove power from all peripheral devices by pressing the POWER OFF pushbuttons and/or placing the power switch in the OFF position for each respective device.

3.5 LOADING SENTRY 400 DEVICE TEST PROGRAMS INTO THE COMPUTER

After applying primary power to the test system, the Disc OPerating SYstem (DOPSY) program is normally loaded into the computer core memory (Table 3-1) by the operator. DOPSY has a repertoire of commands that allows the operator to perform such operations as: assemble or compile a source Sentry 400 device test program and load the Tester OPerating SYstem (TOPSY) program into computer core memory. Instructions for performing these operations are found in the following paragraphs. A repertoire of DOPSY commands is shown in Table 3-10, detailed instruction in their use can be found in the DOPSY manual.

Table 3-10. Summary of DOPSY Commands

Command	Description
JOB	Initializes system for processing a new job by clearing working storage on the disc and resets the Primary Input Device (PID) and Primary Output Device (POD) to the standard system values.
ASM	Assembles a source program read by the PID from a specified device, or from a named disc file. Options to this command will produce assembly and symbol table listings, and generate an object program. At the conclusion of an assembly, the object program is left in working storage.
EXEC	Causes object programs to be loaded from PID, a specified device, disc working storage, or a named disc file; a core image program can also be loaded from a named disc file.
CREATE	Accepts data from a specified device or disc working storage and creates a new file named by this command. If a file by the name specified by this command already exists (i.e., file "n" may have been previously created using the ASSIGN command), the data will be stored in the existing file.
ASSIGN	Allocates the specified amount of space on the disc as a new file named by this command; or changes the amount of space allocated to an existing file by that name.
COMPILE	Compiles a source program written in FACTOR language from a specified device, or from a named disc file. Options to this command will produce listings or object code listings. At the conclusion a compile the data is left in working storage.

Table 3-10. Summary of DOPSY Commands (Continued)

Command	Description
FDUMP	Allows the user to dump the contents of his directory, or a portion thereof, to a specified device or PID; also allows part or all of a named disc file to be dumped to a specified device or to working storage.
DELETE	Allows the user to remove (delete) a named disc file to clear the disc working storage area. Also removes the file name from the directory.
RENAME	Allows the user to rename a specific disc file or to change the job number required to access the files belonging to the current job.
DUMP	Allows the user to dump a specified portion of core memory to a specified device.
NOTE	Allows the user to output the accompanying text, (between quotation marks), to a specified device.
SET	Allows the user to temporarily redefine the PID and POD; effective only until the next JOB or SET command.
PATCH	Allows the user to modify the existing contents of a named core image disc file and/or to add to the data stored in the file, within the limits of the file size as established by the ASSIGN command.
EDIT	Allows the user to modify disc resident programs
TOPSY	Calls the tester operating system.

3.5.1 Loading DOPSY From Disc Memory

The following procedure should be used to load the Disc OPerating SYstem (DOPSY) program into the FST-1 computer core memory from the Model 2060 Disc Memory.

1. Verify that the system power is on and is in the Ready condition. See Section 3.3.

2. Put the two card Disc Bootstrap program followed by a blank card in the card reader hopper (face down with the top edge towards the operator). The Disc Bootstrap program cards must be in the following order: BINARY BOOTSTRAP No. 1, then BCD BOOTSTRAP FOR ARR.

3. Place the card reader in the Ready condition by pressing the following card reader pushbuttons in the sequence listed: POWER ON, START. Wait for READY lamp.

4. At the computer control panel, depress the STOP, RESET, and LOAD CDR (or MT if supplied with system) switches in that order. After the LOAD CDR switch is depressed, the card reader should read the first card of the Disc Bootstrap program, i.e., the BINARY BOOTSTRAP No. 1 card.

NOTE

If the card reader fails to read the card, visually check the status indicators on the card reader control panel. If the card reader is still in the Ready condition, repeat step 4; if a "check" indicator is illuminated, take necessary corrective action to restore the card reader to the Ready condition then repeat step 4.

5. Set the CPU SWITCH REGISTER switches to 01000100_8. Set single instruction Cycle (SIC) and depress LDC (load command register). Then put SIC down and depress START. (The second card of the Disc Bootstrap program "BCD BOOTSTRAP FOR ARR," should now be read; if not, make sure that the card reader is in the Ready condition and repeat step 5.)

6. With the successful completion of step 5, the DOPSY program will be loaded into core memory from the disc memory and an asterisk (*) printed on the Teletype printer to signify that DOPSY is resident in core memory.

7. Initialize the DOPSY system and start a job process by typing the DOPSY command "JOB" using the following format: // JOB 'xxxx' where xxxx is the four character alphanumeric job code, selected by and identifying the originator of a desired repertoire of programs.

3.5.2 Compiling a Source Factor Program

After DOPSY is stored in the computer core memory using the procedure in paragraph 3.5.1, the operator can compile a FACTOR "source" device test program using the DOPSY command COMPILE. If the "source" device test program does not presently reside on the disc as a STRING file, the compilation can be performed in one of two ways:

1. Read and compile the "source" program directly from the desired input device (i.e., card reader, TTR, magentic tape or TTK) and leave an object program in working storage on the disc using the DOPSY command COMPILE. The resultant object program can now be stored as a permanent DATA disc file using the DOPSY command CREATE. (This DATA disc file *cannot* be edited by the EDIOTR program–only STRING files can be edited.)

2. Read the "source" program from the desired input device and create a permanent STRING disc file using the DOPSY command CREATE. (This STRING file can be edited at a later time if desired using the Editor program). The newly "created" STRING file can now be read from the disc and compiled, with an object program left in working storage on the disc, using the DOPSY command COMPILE. The resultant object program can now be stored as a permanent DATA disc file using the DOPSY command CREATE.

The following procedure should be used to compile a source device test program in accordance with method number 2 if the input device is the card reader:

1. Load the source card deck in the hopper face down with the top edge toward the operator.

NOTE

The last three cards in the source deck must be an END, //, and a blank in that order.

Turn the card reader on and place it in the READY condition.

2. Initiate the card reader operation and store the program as a STRING file on the disc by typing the CREATE command as follows:

```
// CREATE 'xxxxxx' STRING CR
```

where 'xxxxxx' is any allowable user defined file name. The cards will now be read and the program stored on the disc. When the operation is finished, the teleprinter will respond by printing an asterisk. See NOTE on CR Error Recovery

The "name" should indicate in some manner, for future reference, that it is a STRING file; Fairchild programmers generally start the name with an asterisk to indicate this, e.g., '*ADDER'.

3. Type the COMPILE command, preceeded by two slashes and followed by the desired compiler options:

e.g., // COMPILE 'xxxxxx' OBJ

where 'xxxxxx' is the file name assigned in step 2. This example causes the resultant object program to be stored in the disc working storage also. The teleprinter will print an asterisk when the operation is complete. Refer to the description of COMPILE in the DOPSY manual for more detailed use of the command and its options. Other options are LIST or LISTOBJ or any combination of the three.

4. Store the object program left in working storage in step 3 as a permanent DATA file on the disc by typing the CREATE command as follows:

// CREATE 'xxxxxx' DATA

where 'xxxxxx' could be the same "name" used in step 2 without the STRING file identifier; e.g., 'ADDER' instead of '*ADDER'. The teleprinter will print an asterisk when the operation is complete.

The following procedure should be used to compile a source device test program in accordance with method number 2 if the input device is the Teletype paper tape reader:

1. Type the CREATE command as follows:

// CREATE 'xxxxxx' STRING TTR

where 'xxxxxx' is any allowable user defined file name.

2. Load the source tape into the Teletype paper tape reader such that the arrows on the tape point toward the operator. Place the Teletype START/STOP/FREE switch in the START position.

3. Press the START pushbutton on the CPU Front Panel; the tape will now be read and the program stored as a STRING file on the disc. When the CREATE operation is complete, the teleprinter will print an asterisk.

4. Type the COMPILE command, preceeded by two slashes and followed by the desired compiler options:

e.g., // COMPILE 'xxxxxx' OBJ

where 'xxxxxx' is the file name assigned in step 1. This example causes the resultant object program to be stored in the disc working storage area. The teleprinter will print an asterisk when the COMPILE operation is complete.

5. Place the Teletype START/STOP/FREE switch in the FREE position.

6. Store the object program left in working storage in step 4 as a permanent DATA file on the disc by typing the CREATE command as follows:

```
// CREATE 'xxxxxx' DATA
```

The teleprinter will print an asterisk when the CREATE operation is complete.

Although it is possible to compile a device test program entered via the Teletype keyboard, the length of most device test programs would make this a cumbersome method. Therefore this method will not be discussed here.

A program may be compiled directly from the source (cards, paper tape, keyboard) by typing

```
// COMPILE OBJ CR
// CREATE DATA 'xxxxxx'
```

This does not create a source file on the disc and hence may conserve disc space. However, source EDIT will not be possible.

3.5.3 Loading TOPSY From Disc

After the Sentry 400 device test program has been compiled and stored as a permanent "data" file on disc memory the TOPSY (Tester OPerating SYstem) program is loaded into core memory from the disc memory as follows:

1. Type // TOPSY on the teletype keyboard. The DOPSY program will now load TOPSY into core memory from the disc memory.

NOTE

If DOPSY cannot locate TOPSY on the disc, the error message "ERROR—FUNCTION NOT IMPLEMENTED" will be printed and the system will return to a "wait-for-DOPSY-command" state. If TOPSY is loaded but the TOPSY monitor determines that a TOPSY subroutine is missing (e.g., data logger or command processor), the error message "ERROR SYSTEM 11" is printed, DOPSY is automatically reloaded, and an asterisk (*) is printed when DOPSY is resident in core memory.

3.5.4 Loading Device Test Program From Disc Using TOPSY

After the Tester OPerating SYstem (TOPSY) program is resident in core memory the device test program is loaded into core memory from the disc memory as follows:

1. Press the MON pushbutton–TTY will respond with a colon ":".

2. Type /. LOAD 'xxxxxx' STATI where 'xxxxxx' is the name of the desired test program as it appears in the disc directory under the current job number and I is the station number assigned to execute the program. TOPSY now searches for and (as far as the operator is concerned) loads the named test program; when the LOAD operating conditions (See 3.5.5) and then start testing.

NOTE

The named device test program must be type DATA (refer to preceeding paragraphs).

After the device test program is resident in core memory, along with TOPSY, the operator can commence testing immediately, or initialize or modify the tester operating conditions (e.g., change test delay) and then start testing.

3.5.5 Initialize or Modify Tester Operating Conditions with TOPSY Monitor Commands

Prior to the start of active device testing using the device test program currently resident in core memory along with TOPSY, the operator may wish to initialize or modify the tester operating conditions using any or all of the TOPSY monitor commands available. A brief description of each command is found in Table 3-11 ; refer to the TOPSY Manual for a detailed description and format options for each TOPSY command.

Table 3-12 gives a few examples of the format statements acceptable for TOPSY commands, beginning with the loading of a device test program. In the examples all noise words are ignored by the computer. A noise word is defined as a word or name other than those reserved names recognized by the command which may be inserted freely in the command statement to improve readability.

NOTE

Each TOPSY command must be preceeded by "/." (slash-period) and end with a STATI (Station number).

Table 3-11. Summary of TOPSY Commands

Command	Description
LOAD	Initializes the tester (equivalent to depressing tester RESET switch) defines the name of the object test program to be loaded into core memory from disc memory when the Station Start Switch is depressed. The modifications to the tester operation (performed with commands MODIFY, PAUSE, DATALOG, TITLE, and SWITCH) are cleared by this command unless SAVE is specified when loading.
TITLE	This command normally follows a LOAD command; it allows the operator to enter a message ≤64 characters which will be stored internally by TOPSY until required. The TITLE message will be printed at the top of the first page of data log information each time a test program is executed following the TITLE command.
PAUSE	Initializes the data logger subroutine such that testing will pause (halt) upon detecting each failure after the START switch is depressed while in the AUTO mode; PAUSE can also be used to initialize the interpreter subroutine such that testing will pause (halt) after executing a specified statement number. In both cases, testing is resumed after depressing the START switch on the appropriate test station.
MODIFY	This command allows the operator to specify a new test delay. The original test delay instructions in the test program are ignored, not destroyed, and can be reinstated by turning the MODIFY condition off with another MODIFY command or with a CLEAR command.
DATALOG	This command initializes the datalogger subroutine such that datalogging is accomplished in accordance with the command options.
SET	This command allows the operator to temporarily specify a new primary input or output device until changed by another SET command. This command does not need to be followed by a station number.
SWITCH	This command allows the operator to specify a floating point number which is stored in the floating point global variable SWITCH. The global variable is used with appropriate Sentry 400 Users Language instructions to automatically control the device test program execution sequence.
CLEAR	Execution of this command rescinds all modified conditions established by the preceding commands; i.e., TITLE, PAUSE, MODIFY, DATALOG, and SWITCH.
DOPSY	Execution of this command resets the Tester, stores TOPSY in its present state on a disc file, then loads the DOPSY program into core memory from the disc memory. This command does not need to be followed by a station number.
SYNC	Causes a sync pulse at the test station panel jack to occur at the specified statment number.

Table 3-12. TOPSY Command Format Examples

```
/.    LOAD 'DTL4X' STAT2
/.    CLEAR STAT2
/.    TITLE '3/4/69 RUN NO. 15 ARRAY TYPE 944Q' STAT2
/.    DATALOG ON LP ALL FCT DCT AND MEASURE STAT2
/.    SET LP AND CR
/.    SWITCH 5 STAT2
/.    PAUSE ON FAIL STAT2
/.    PAUSE ON STATEMENT 15 STAT2
/.    MODIFY ON 3.5E-6 SECONDS STAT2
```

3.5.6 Initiation of Active Device Testing

Assuming the necessary software programs, i.e., TOPSY and the desired device test program, are resident in the CPU core memory and the tester operating conditions have been initialized (refer to preceeding paragraphs), the user is now ready to insert a prewired load board if desired and connect the corresponding device to be tested into the test head and commence active testing.

Testing with the Sentry 400 can be done without a load board. The programmable power supplies are routed to the I/O connector and the user may wire his test socket or probe ring to the appropriate pins. Functional testing can be made with no load on outputs, however, while making DC parameter measurements on outputs, the PMU can force load currents.

The load board may be used for the following applications:

1. DUT has open collector outputs requiring external pullup resistors.

2. Functional tests are performed with output pins under load.

3. Power supply pins are to be addressable under program control.

4. User requires other special circuitry such as recirculation logic for high speed shift register testing, etc.

3.5.7 Preparing Performance Board for Testing

Figure 3-10 shows the layout of a universal performance board provided by Fairchild Systems Technology. Five load boards are provided per each 30 pin configuration. The contact pins of the load board, when inserted into the load board socket, are connected in parallel with the corresponding 30 pins of the tester. At the load board socket the force and sense (utility) lines are laid out in two rows. Between the force and sense lines are patch plugs and receptacles for solderless connection of components (1 watt resistor lead sizes).

DPS1, DPS2, and DPS3, also EB0, EB1, EC0 and EC1 are brought out to the load board and connected as desired. The +5Vdc and ground may also be connected to the pins as desired.

The user may stuff every pin of a load board with resistors connected to the utility lines and use one board for a whole family of device types since the utility lines may be switched under program control.

After the user has debugged a new device program it is suggested that a new printed circuit load board be constructed for that particular device or family. The user will gradually build up a library of load boards. These boards should be easy for the user to fabricate for the tolerances are very wide, i.e., the edge pins are on 0.2 inch centers.

Figure 3-11 is a simplified schematic showing the association between the load board pins and tester pins. Figure 3-12 thru 3-16 illustrate some of the many possible ways in which the load board can be used. If further assistance in the use of these load boards is required, please consult your local Fairchild representative.

The final step in wiring a performance board for a specific device type is to identify that board so it is used only with the device type intended. This is done by wiring the SID (socket identification) terminals 0 through 14 for a discrete 15 bit binary code, with SID 0 being the least significant bit of the code. A terminal tied to ground represents a binary "0," while an open terminal represents a binary "1." This hard wired code can be checked by a user programmed statement in the device test program, causing the test program to halt if the hardwired code and the programmed SOCKET ID number do not compare.

3.5.8 Inserting Performance Board and Device into Tester

Following the wiring of a performance board for the specific device, the performance board and device to be tested may be inserted into the tester.

The performance boards are inserted through the narrow access doors in the tester side doors. The load board for the first 30 pins (i.e., pins 1-30) is inserted into the bottom right hand load board socket and the load board for the second set of 30 pins (i.e., pins 31-60) is inserted into the bottom left hand socket. Two similar sockets are located on the upper left and right side of the tester for the next two groups of 30 pins.

Following the insertion of the load boards, the user may connect his probe ring or test socket to the appropriate I/O pins on the tester. The device to be tested may now be inserted into the test socket and the device is now ready for testing.

3.5.9 Select Test Mode and Commence Testing

If all instructions in the preceeding paragraphs have been executed in the proper sequence, the Tester OPerating SYstem (TOPSY) program and device test program are resident in core memory, the proper performance board is in place and the device to be tested in inserted in the test socket. The operator may now select the desired test mode of operation and commence testing as follows:

1. Set the MAN switch on the Test Station Front Panel for the desired mode of operation i.e., AUTO or MANUAL. The button will be illuminated for manual and will be off for automatic. TOPSY MONITOR COMMANDS and the test mode.

2. Depress the test station START switch. The device test program will now be executed under program control according to the conditions established by the TOPSY MONITOR COMMANDS and the TEST MODE switch.

3.5.10 Error Messages

When an error is detected the compiler will always type the full current record. For the most part FACTOR's error messages are self-explanatory; they are listed below with some comments. The error message text begins at the left margin. An upward pointing arrow indicates the position in the source statement analysis at which the error was found.

When an error is detected one of two procedures is taken. If the error is recoverable, i.e., if the compiler can continue, FACTOR will continue to compile and notify the user of further errors. If the error is not recoverable, the DOPSY monitor will be called and an asterisk will be typed to notify the user that he is back in monitor. The user then has the option of correcting errors in the source program and redoing the compilation, or, if the program compiled error free, he may save the object program by creating a data file on the disc.

The text of the messages MISSING)) and]] have doubled up on the parens and brackets because the up arrow error position indicator might be placed within the error message text and make the message unreadable if only one paren or bracket was specified and then replaced with up arrow.

Examples:

```
MISSI↑G ))
MISSING ↑)
MISSING )) ↑
```

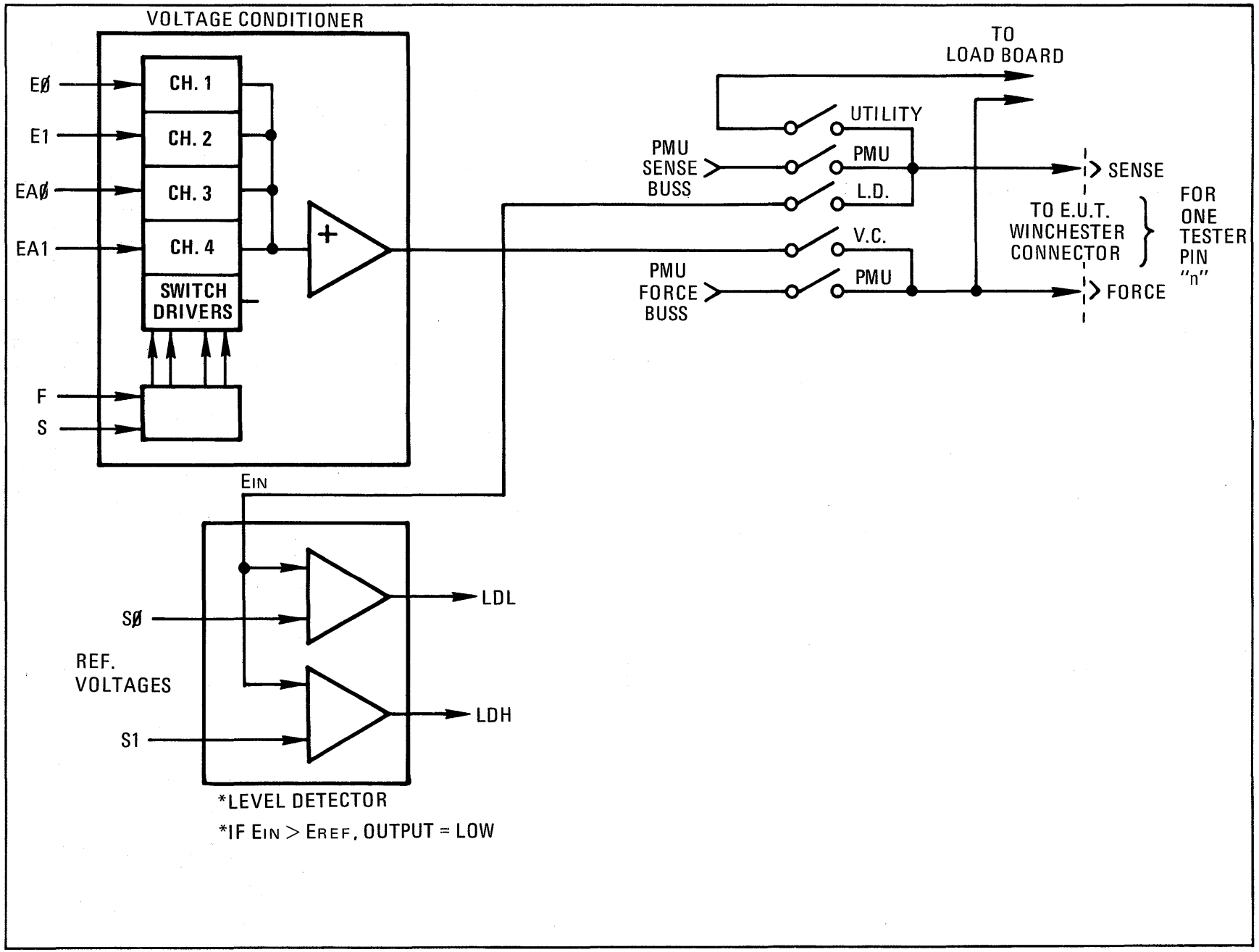

Figure 3-11 Simplified Tester Schematic

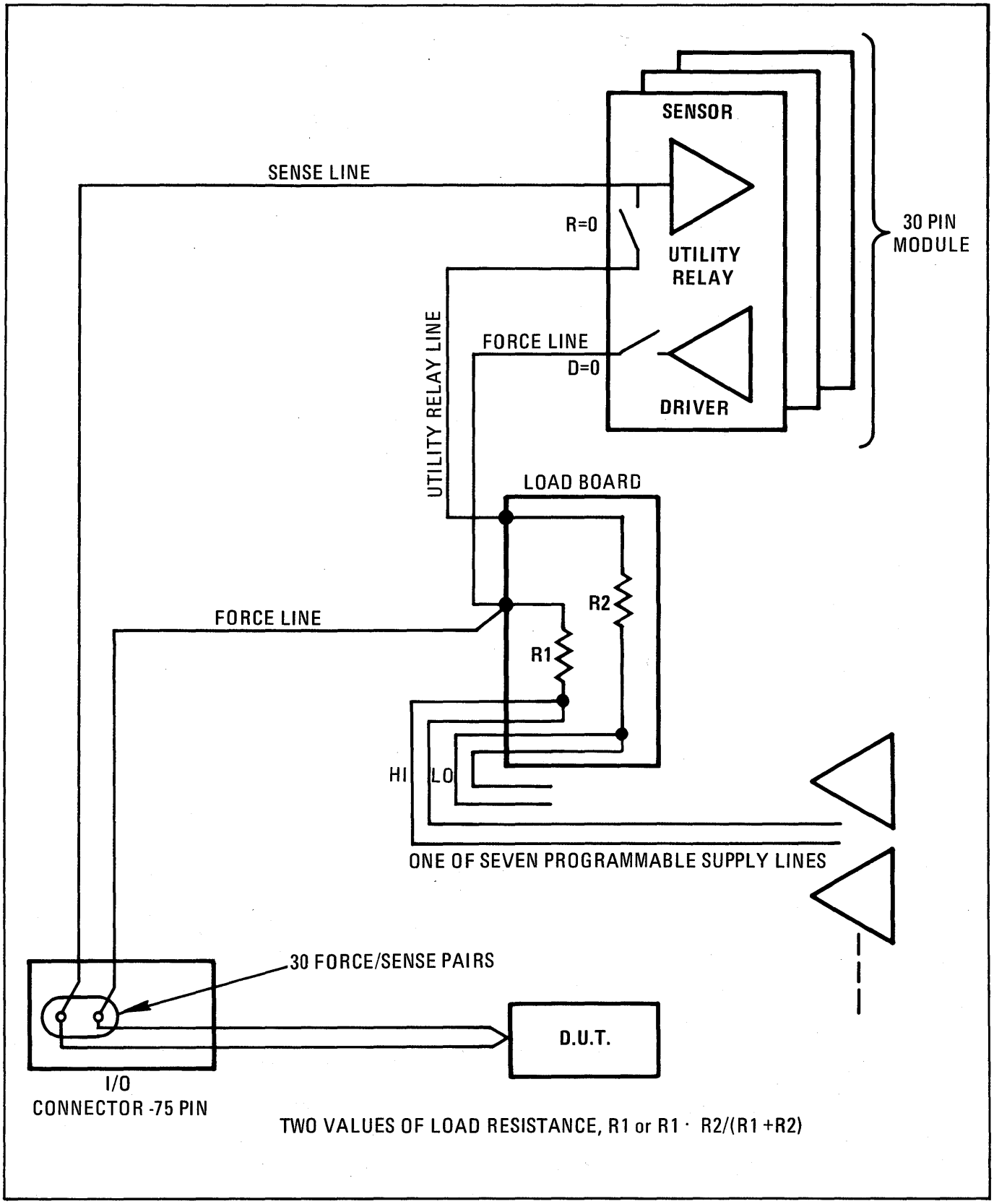

Figure 3-12 Load Board, Two Values of Load Resistance

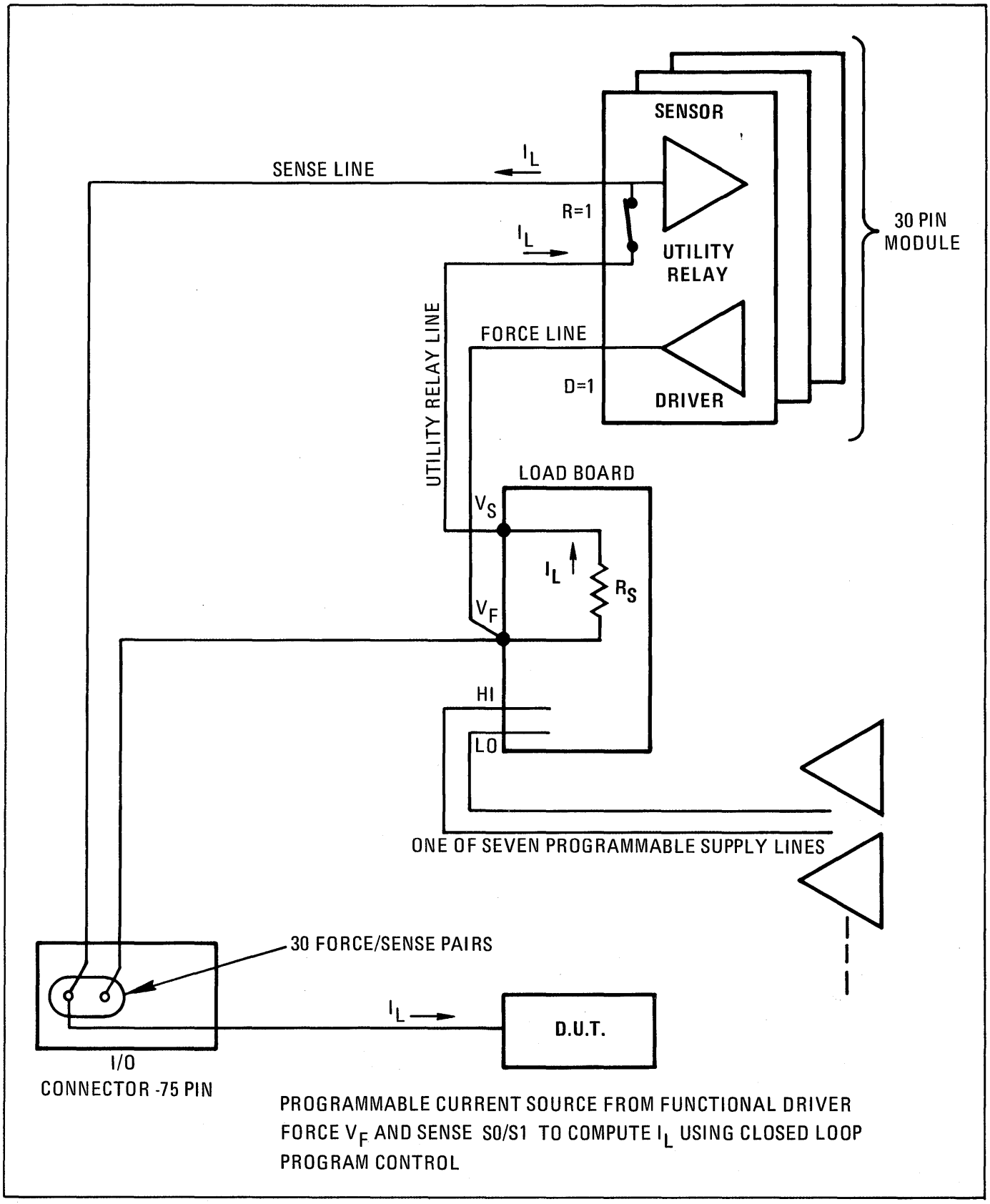

Figure 3-13 Load Board, Programmable Current Source

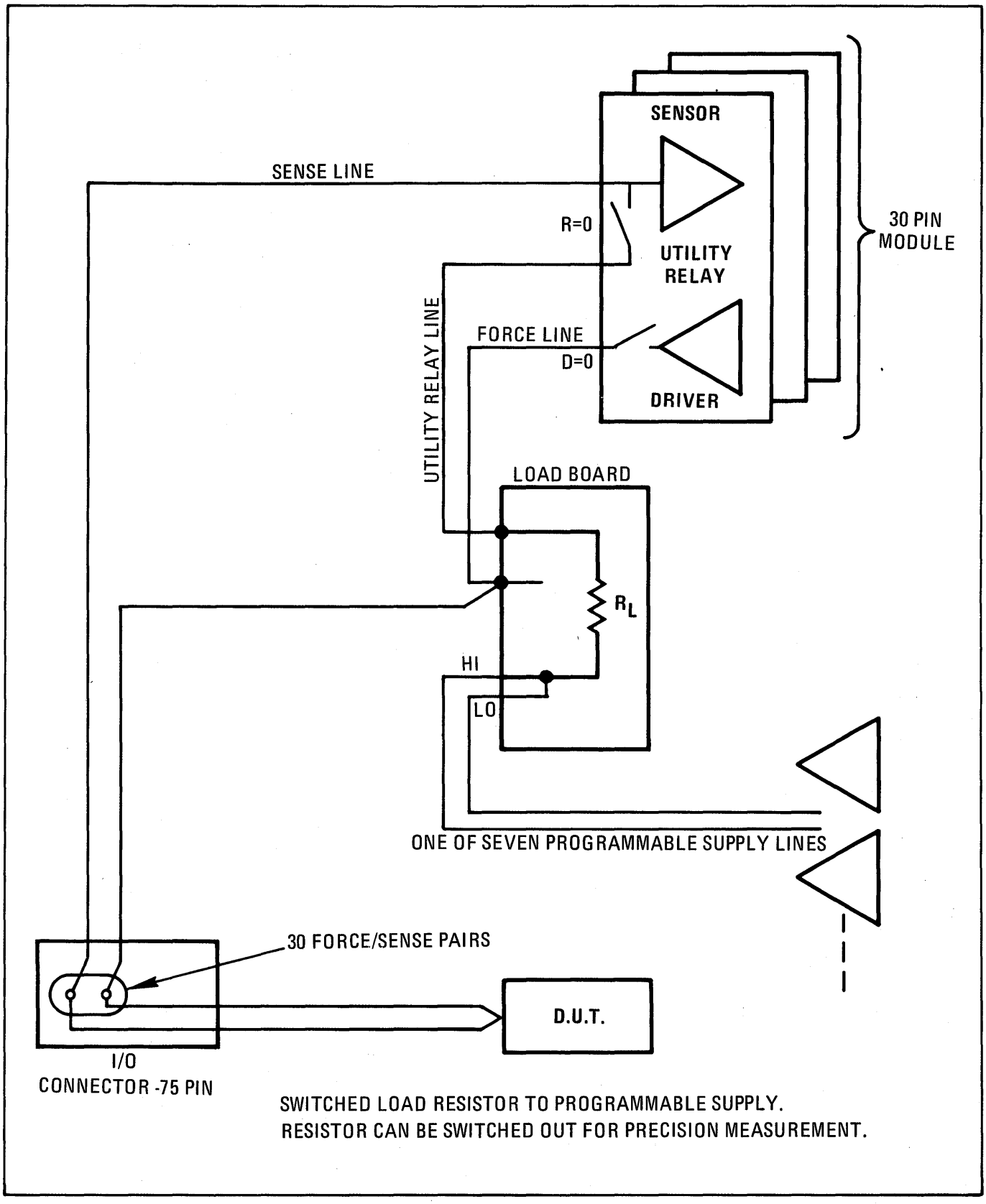

Figure 3-14 Load Board, Switched Load Resistance

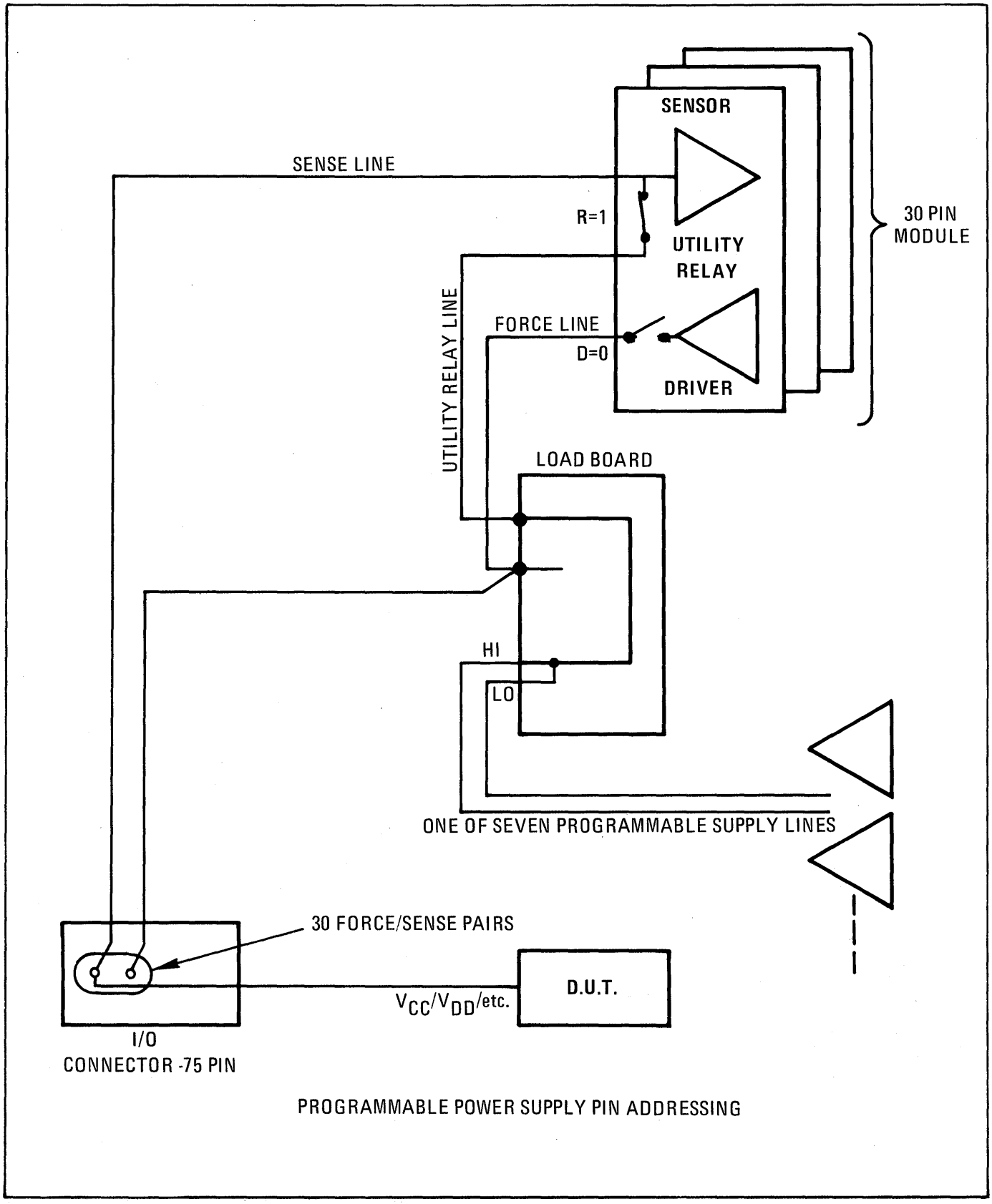

Figure 3-15 Load Board, Programmable Power Supply

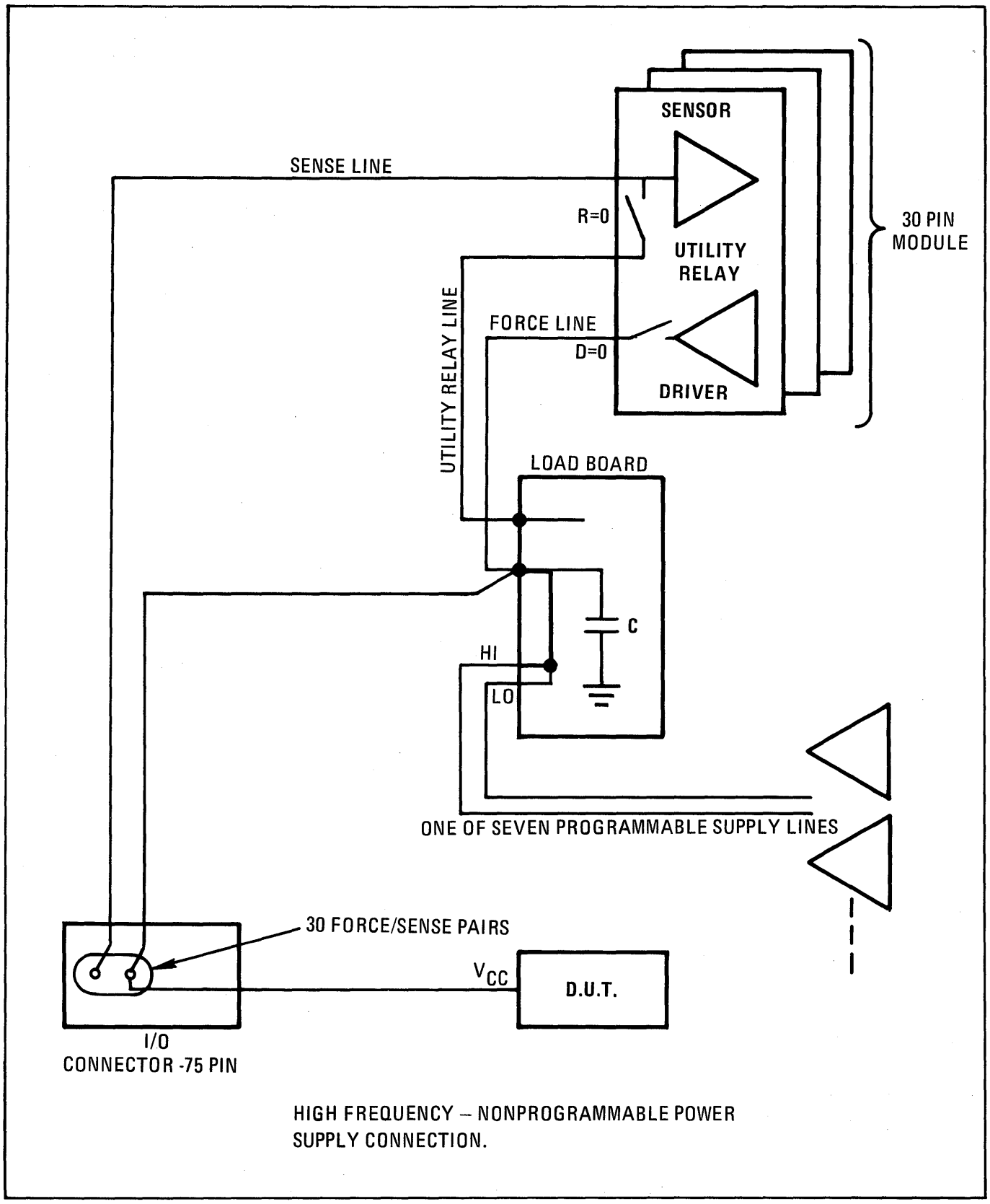

Figure 3-16 Load Board, High Frequency

Table 3-13. Error Messages

Error Text	Definition
"VARIABLE NAME" DEFINED PREVIOUSLY	Notifies user of duplicate label definition within the same block.
"VARIABLE NAME" IMPROPERLY USED	A label has been referenced which has not been defined or a mistake in logic has been detected like the use of a variable as a scaler when it has been defined as an array.
SEQUENCE ERROR	An error has been found in the sequence numbers punched in the source card deck after column 72. The statement is still compiled correctly.
SS FUL	The compilers capacity for storage of symbols has been exceeded. Reduce number of symbols used.
NW FULL	Too many noise words.
WORK FULL	Program has a compound tail too large to be processed as one statement. The program should be broken into Blocks or Subroutines.
EXIT FULL	Same as above.
DISC OVERFLOW	There is not enough space on the disc for further object program to be built up in working storage.
TOO MANY NESTED BLOCKS	There are more than 8 total blocks nested within the program.

Table 3-13. Error Messages (Continued)

Error Text	Definition
INVALID TERMINATOR	An expected terminator or delimiter is incorrectly specified or missing.
I/O SPECIAL ERROR	The I/O control word has indicated an error.
END OF FILE INPUT	The input file has been exhausted without finding an END statement.
TOO MANY VARIABLES	A block has been specified with more than $127_{(10)}$ variables.
SYSTEM 2 ERROR	Working storage overflow signal.
PROGRAM TOO BIG	The program has more than $1{,}000{,}000_8$ instructions.
MISSING))	A left or right paren has been left out.
EXPRESSION SYNTAX	An expression has been written incorrectly.
MISSING]]	A left or right bracket has been left out.
MISSING NAME	An identifier should have been specified in this syntactical position.
MISSING NUMBER	A number should have been specified.
STATEMENT SYNTAX	A statement has been incorrectly written.
STATEMENT TERMINATOR	A syntactical delimeter or a semicolon is missing.
NUMBER SYNTAX	A number has been specified incorrectly.

3.5.11 Editing FACTOR Programs

The following paragraphs describe a method of using the teletype for editing a program. An alternate method is to type each step of the edit procedure on individual punch cards and process the cards through the card reader.

The Sentry 400 edit program is resident on the disc and can be called upon through the DOPSY monitor. The edit program allows editing of any STRING files on disc or the combining of two or more string files. Object programs cannot be edited by the EDITOR program; only source program STRING files can be edited. The EDIT program takes the STRING file named in the OPEN statement and copies it under control of the EDIT routines to working storage. After editing is complete, and the string files has been completely copied into working storage, the edited file can be added to the disc permanent file. A repertoire of EDITOR commands is shown in Table 3-14; detailed instructions in their use can be found in the UTILITIES Manual.

NOTES:

1. In order to prevent multi-versions of the same file, DELETE the old file and CREATE a new file using the same file name.

2. Number Representation:

   NN is a decimal number.
   NNB is an octal number.

   Editor will assume any number with suffix B as OCTAL, otherwise decimal.

   Example:

10	decimal number
10B	octal number

3. The Editor is terminated, giving control to the DOPSY monitor, by typing // while the Editor is awaiting a new command.

4. After terminating the Editor, the STRING file left in W.S. can be stored as a permanent STRING file using the create command as follows:

   // CREATE 'new file name' STRING

To edit a program, DOPSY must first be called into memory from the disc, this is achieved as follows. (Assuming DOPSY is being called from TOPSY)

1. Type /. DOPSY↓ on the teletype keyboard. The DOPSY program will now be loaded into core memory and the teletype will respond with an * (asterisk) (See Table 3-14)
2. Following the * of step 1, type: // EDIT. The '// EDIT' informs DOPSY that editing is to be performed. The teletype will respond with: >

Table 3-14. DOPSY Edit Program Commands

Command Name	Form(s)	Definition
OPEN	0 'file name'	Open the named file as the OLDFILE for editing purposes.
COPY	CEOF	Copy to end of file.
	CNN/NNB	Copy NN records to new file in working storage.
	C LABEL	Copy all records from old file through record with label.
	C LABEL + NN	Copy through the label plus NN number of records.
	C	Copy next record.
	CARRIAGE RETURN	Copy next record.
	COPY	Copies the file named, record by record to working storage. The last record moved to working storage is printed on the TTY. LABEL = the first 8 or less characters in the first eight positions of the record. NOTE: If label is not found, editor will copy to the end of the input file.
DELETE	D	Pass over next record without copying into W.S. Record deleted is printed.
	Dnn	Pass over next nn records without copying into W.S. (The last record deleted is printed on the TTY.)
BACKUP	B	Back up one record.
	Bnn	Back up nn records in both input and output files. (Printed on the TTY is the last record copied to the output file.)
INSERT	I	Take the following records, until terminated by a '//' record, as STRING input to W.S.
SET	SCR	Change input device to card reader.
	STTK	Change input device to Teletype Keyboard.
ALTER	A	Pass over next record without copying into W.S.; then allow insertion of one or more records, until terminated by // record, as STRING input to W.S. Record to be altered is printed on TTY.

Table 3-14. DOPSY Edit Program Commands (Con't)

Command Name	Form(s)	Definition
	An	Pass over next n records without copying into W.S.; then allow insertion of one or more records, until terminated by // record, as STRING input to W.S. Last record passed over is printed on TTY.
XOUT	X	Delete last record from the W.S. output file. Last record in output file is printed on TTY.
	Xnn/nnB	Delete the last nn records from the W.S. output file. (Printed on the TTY is the last record remaining in working storage after execution of the command.)

3. Following the > in step 2, type O 'file name'↓. This statement informs the EDITOR to open the named file for editing. The teletype will respond with a >.

4. Assume that the named file, now open, has 100 octal statements and the operator wishes to delete statement number 50 (octal). Immediately following the > in step 3, type C47B↓ (i.e., copy the first 47 octal statements into working storage). The teletype will respond with the last record copied to W.S. and a >.

5. Following the > in step 4, type D↓ (i.e., delete or pass over the next record without copying into working storage). The teletype will respond with a >.

6. Assume that after step 5, a new record is to be inserted after record 75. (Up to the present time 47 octal records have been transferred to working storage.) Type after the > in step 5, C25B↓ (i.e., copy the next 25 octal statements into working storage). The teletype responds with a >.

7. Following the > in step 6, type I↓ (i.e., take the following records until terminated by a '//' as STRING input to wroking storage.)

8. After the carriage return in step 7, the teletype responds with an = and waits for the new record to be typed. Assume the new record is FORCE VF1 4.3 VOLTS, RNG2;. TTY responds with an =. Type //↓ after the = (The // terminates the insert command to the editor.) The teletype responds with a >.

9. After the > of step 8, type CEOF↓ (i.e., copy to end of old file). The teletype responds with EOF - INPUT, then does a carriage return and line feed and prints >.

10. After the > of step 9, type //↓ (The // terminates the editor and restores control to DOPSY monitor.) The teletype responds with an *.

11. The next step is to create a new string file of the records in working storage. This is achieved by typing the following after the * of step 10.

    // CREATE 'new file name' STRING. The teletype will respond with an *.

12. The last step is to delete the old file. This is achieved by typing the following after the * step of step 11.

    // DELETE 'old file name'.

The following Table 3-15 shows the teletype printout of the 12 steps just described.

Table 3-15. DOPSY Editor Printout

```
STEP    1     /. DOPSY↓
        2     * // EDIT↓
        3     > 0 'file name'↓
        4     > C47B↓
                (Re: Last record copied to output file)
        5     > D↓
        6     > C25B↓
        7     > I↓
                (Insert record in output file here)
        8     = //↓
        9     > CEOF↓
              EOF-INPUT
       10     > //↓
       11     * // CREATE 'new file name' STRING;
       12     * // DELETE 'old file name';
```

A further important feature of the Sentry 400 EDITOR program is the BACKUP command.

If it is necessary to backup only a few records, the backup command is quite effective. On the other hand, if the operator has edited all the way down to record 98 of a 100 record program and then discovers it is necessary to edit an error in record 2, the backup method should not be used because editing between record 2 and 98 would be overlaid and therefore lost. The easiest method would be to continue editing from the current record, create a string file, then reopen the file and correct the error.

If the backup command is to be used, the following method is recommended. Assume that after step 8 (75 records have been copied into working storage) the operator realizes that an error still exists in record number 73. After the > of step 8, the operator types Bnn (the B informing the editor to backup and make the previous nn records available for reprocessing). In this particular case, since the current record is record 75 and the operator wishes to backup to record 73, the operator should type B2. (75-73). The teletype responds with a >. After the >, the operator may use the DELETE, INSERT, or ALTER statement to perform the required operation as shown in Table 3-14. *If the records through which the backup statement was used contained editing, this editing must again be performed.*

Section IV
Programming

4.1 INTRODUCTION

The Sentry 400 Computer Controlled Test System is controlled by the FST-1, a general purpose digital computer. The sequence of operation is dependent upon programmed instructions and statements resident in the CPU core memory.

Two programs must be resident in core memory before device testing can be performed. The first, is referred to as TOPSY (Tester OPerating SYstem program). The individual TOPSY instructions are normally of no concern to the user; however, it is possible to modify the tester operation as determined by TOPSY with a repertoire of TOPSY command statements entered via the teletype or card reader.

The TOPSY program will cause the CPU to execute the statements of the second program, a device test program. The device test program consists of a number of statements written in FACTOR language that is very similar to FORTRAN. The statements consist of a combination of English language words, abbreviations, and mathematical statements that are descriptive of the operation to be performed by the tester.

The Sentry 400 Test System is capable of being programmed to automatically perform two distinct types of tests, functional tests and DC measurements. These tests are performed on digital networks such as: large scale integrated arrays (LSI), complex integrated circuits, printed circuit boards, and other digital subsystems.

The Sentry 400 performs functional tests on devices that contain up to as many as 240 input/output logic pins. There are no restrictions on programming the division of logic pins between inputs (to the device-under-test) and outputs (from the device-under-test); i.e., it is possible to program all pins as inputs, as outputs, or as any combination of the two up to the maximum of 240 pins.

The structure of the FACTOR Language is such that during the course of a functional test program, any signal pin can be redefined from an "input" pin to an "output" pin, and vice versa. It can also be redefined from a "don't care" terminal to a "care" terminal, and vice versa. The "don't care" condition is useful, for example, to ignore specified output pin conditions if limited interim tests are being performed while the internal states of a device are being set to a known condition. Redefining a signal pin as an "input" pin or an "output" pin may be useful, for example, when testing a device that has bidirectional terminals.

Additional FACTOR statements allow the user to specify DC measurement parameters for tests such as: force a voltage on pin "n" and measure the current, or force a current on pin "n" and measure the voltage.

In addition, the magnitudes of all the test system reference voltages and currents such as device supply voltages, functional logic level forcing levels, and the Go/No-Go threshold levels are programmable, as are the internal comparator strobes, synchronous sync signals, and the system test delay.

4.2 TESTER STATEMENTS, GENERAL DESCRIPTION

A summary of the Sentry 400 Tester Statements is found in Table 4-1. For more detailed information on the exact format variations, refer to the FACTOR (Fairchild Algorathmic Compiler Tester ORiented) manual.

Table 4-1. Sentry 400 Tester Statements Summary

Statement	Description
SET DELAY,DC	Executing this statement presets the time delay for subsequent execution of DC tests; i.e., when executing a FORCE PMU or FORCE VOLTAGE/CURRENT statement. Executing SET DELAY without the modifier, "DC," presets the strobe delay for subsequent execution of functional tests; i.e., when executing a SET F statement.
SET S1/S0	Sets the comparator "1" or "0" reference power supply to the value specified.
SET CLOCK	Specifies the number of clock (sync) signals that the tester outputs during functional tests.
SET PMU SENSE/FORCEV/ FORCEI,RNG/AUTO	The 'SET PMU SENSE, RNG' form of this statement initializes the PMU for a measurement in the specified range. It is normally used in conjunction with a 'FORCE VOLTAGE/CURRENT' statement, or a 'SET PMU FORCEV/FORCEI, RNG' statement. The 'SET PMU FORCEV/FORCEI, RNG' form of this statement initializes the specified range before an accompanying 'FORCE PMU' statement is executed. AUTO sets the automatic ranging to best resolution for force or sense.
SET LOGIC POS/NEG	This statement initializes the functional test comparator logic pass conditions for either positive or negative logic. Positive Logic is assumed unless otherwise specified.
SET D	Set each tester pin in the specified rank to the defined input or output pin configuration.

Table 4-1. Sentry 400 Tester Statements Summary (Continued)

Statement	Description
SET F	Set the input forcing logic state ("1" or "0") for those pins in the specified rank programmed as Inputs, and the expected logical output state for those pins programmed as Outputs.
SET M	Set the "care" (comparison enable) or "don't care" (comparison disable) for each pin in the specified rank.
SET S	Select which set of input reference supplies (E0/E1,EA0/EA1, etc.), are to be used to force the input voltage on each pin of a specified rank.
SET R	Open or close the utility relay associated with each pin of a specified rank.
ENABLE ILO/IHI/VLO/VHI	Two ENABLE LIMIT statements are used to specify the upper and lower limits against which all following programmed current/voltage forcing statements are compared; programmed V_F/I_F statements within these limits are executed, while statements outside these limits cause a terminal error.
ENABLE CLOCK	Enables circuitry in the test head so that clock pulses from SYNC jacks on the front panel will be connected to tester pins 1, 2, 3, and/or 4 as specified.
ENABLE STROBE	Enables the functional test comparator strobe to be controlled by the contents of F Register bits 0-3 and the corresponding bits of this statement. This is used in conjunction with DISABLE COMPARATORS.
ENABLE TRIP LT/GT	Enables the current trip detector of the corresponding voltage forcing unit DPS1, DPS2, DPS3. If the source/load current of the forcing unit exceeds the enabled trip value during a test sequence, program control is transferred to the instruction specified by the "ON TRIP" statement.
ENABLE TRIPV LT/GT	Enables the voltage trip detector of the corresponding DPS supply and puts it in the current force mode.
ENABLE/DISABLE LATCHES	The DISABLE LATCHES form of this statement initializes the functional test control so that the C Register is cleared prior to strobing the functional test comparators for each functional test. The disable mode is assumed unless otherwise specified.

Table 4-1. Sentry 400 Tester Statements Summary (Continued)

Statement	Description
	The ENABLE LATCHES form of this statement initializes the functional test control so that the C Register is not cleared prior to strobing the functional test comparators, thereby retaining a history of functional failures for each tester pin throughout a test sequence.
ENABLE/DISABLE COMPARATORS	The ENABLE COMPARATORS form of this statement initializes the functional test control logic so that the comparator outputs will be strobed to the C Register for each functional test. The enable mode is assumed unless otherwise specified. The DISABLE COMPARATORS form of this statement initializes the functional test control logic so that the comparator outputs will not be strobed to the C Register for each functional test. (Unless ENABLE STROBE matches the F register).
ENABLE/DISABLE RELAY	The DISABLE form of this statement initializes the pin address control logic such that the voltage conditioner for pin "n" will be automatically disconnected before the PMU is connected to that pin. Disable is assumed unless otherwise specified. The ENABLE form of this statement initializes the pin address control logic such that the voltage conditioner for pin "n" will remain connected even though the PMU is connected to that pin; after the PMU is connected to pin "n," the voltage conditioner can be disconnected by executing the DISABLE form of this statement.
ENABLE/DISABLE DCT	The ENABLE forms of this statement define "window" comparison trip limits which establish the "pass" region for all subsequent DC measurements resulting from the MEASURE statement. The DISABLE forms of this statement disable the comparison limits and inhibit the DC fail, regardless of the measured value.
FORCE E	This statement forces the specified voltage conditioner reference supply to the programmed value. If the range is not specified, then the lowest range is automatically set.

Table 4-1. Sentry 400 Tester Statements Summary (Continued)

Statement	Description
FORCE VF	This statement forces the specified programmable voltage Forcing supply (DPS1, DPS2, or DPS3) to the defined value, and automatically connects the supply to the test head load board.
FORCE IF	This statement forces the specified programmable DPS supply to force a current to the defined value. It must be preceded by an ENABLE TRIPV statement.
CPMU PIN	This statement connects the PMU to the specified pin number. Tester pins are specified by values from 1 to 120_{10}. For diagnostic purposes, various internal nodes can be connected to the PMU by specifying a pin number between 128_{10} and 255_{10}.
FORCE VOLTAGE/ CURRENT	This statement forces a programmed voltage or current via the PMU to the tester pin specified by the previously executed CPMU PIN statement.
FORCE PMU	This instruction is used in conjunction with the conditions established by a previously executed "SET PMU FORCEV/FORCEI, RNG;" statement; i.e., the "SET PMU---" statement establishes the FORCE, VOLTAGE/ CURRENT, and RANGE conditions for a DC measurement, while the FORCE PMU statement specifies the numeric value to be forced. When executed, this statement forces a current or voltage as specified, at the tester pin specified by a previously executed CPMU PIN statement.
FORCE STROBE	This statement forces a single functional test strobe (even though the comparators may have been disabled by a DISABLE COMPARATORS statement) thus strobing the comparator outputs to the C Register.
FORCE CLOCK	This statement forces a single clock pulse to occur simultaneously at each of the four front panel SYNC output jacks.
FORCE RESET	This statement forces the test system into the reset state, thus clearing all programmable test conditions.
FORCE DELAY	This instruction forces a time delay to occur prior to executing the next instruction; this delay is directly dependent upon the "tester delay" established by the last SET DELAY statement executed.

Table 4-1. Sentry 400 Tester Statements Summary (Continued)

Statement	Description
XPMU PIN	This statement disconnects the PMU from any tester pin or internal node.
XCON VF1/VF2/VF3	This statement disconnects the specified voltage forcing unit (DPS1, DPS2, or DPS3) from the test head load board after automatically setting the output voltage of the unit to zero volts.
MEASURE VALUE/ NODE, LOG	Execution of this statement causes an analog-to-digital conversion within the PMU of a DC voltage or current at a tester pin or an internal monitor node point. The "MEASURE VALUE" form of this statement is for a DC measurement on the tester pin (i.e., pins 1 through 120) connected to the PMU; the measurement conditions must be preset by a "SET PMU SENSE, RNG" statement. The "MEASURE NODE" form of this statement causes a measurement of an internal monitor node point. The measurement conditions are automatically invoked and will not be affected by such statements as referred to by the "MEASURE VALUE" form. The modifier ",LOG" causes data logging of the measured value according to the conditions established by the TOPSY MONITOR logging command "DATALOG".
ON DCT	This statement establishes program branch control conditional on DC test failures (DCT); it is used in conjunction with, and executed prior to an "ENABLE DCT" statement.
ON FCT	This statement establishes program branch control conditional on functional test failures (FCT).
SET CLAMP POS/NEG/SYM	Sets the PMU voltage clamp levels. The POS selection allows voltages less than the specified value and greater than -0.7 volts. The NEG selection allows voltages greater than the negative of the specified value and less than +0.7 volts. The SYM selection allows voltages between ± specified value.
ON TRIP	This statement establishes program branch control conditional on current trip failures (TRIP). It is used in

Table 4-1. Sentry 400 Tester Statements Summary (Continued)

Statement	Description
	conjunction with and executed prior to an "ENABLE TRIP" statement; i.e., if current trips are enabled and a current trip failure occurs, program control will branch to the statement label specified by this statement.
SOCKET ID	Execution of this statement causes the hardwired identifier code on the performance board in the test head socket to be compared with the identifier code specified. If the two codes do not compare, a system terminal error is issued and the program is aborted; a true comparison allows the program execution to continue.

4.3 PROGRAMMING PROCEDURES

In the following paragraphs, an attempt is made to illustrate to the reader how to use the Sentry 400 Tester Statements that are described in paragraph 4.2. Initially, typical ways of implementing preliminary tester setup, functional tests, and DC tests will be shown. Finally, an actual device test program is presented; it is used to show the reader how a typical device test program could be written to perform both functional and DC testing.

4.3.1 Preliminary Tester Setup Statements

Preliminary tester setup would normally include such operations as: verify that the load board used with the device test program resident in core memory is in the test head socket; establish "window" limits that all programmed current/voltage forcing statements will be compared against; establish a current trip limit for the Vcc power supply, force the Vcc supply to a specified value, then measure the Vcc current and compare it to a programmable limit; force the voltage conditioner logical "0" and "1" reference supplies to specified values; and force the comparator logical "0" and "1" reference supplies to specified values.

Assume the following test parameters for a device to be tested:

1. Vcc = +5.0V, with current limiting $>$ 1mA and $<$ 80mA

2. Voltage conditioner reference supplies:

   "0" = +0.5V
   "1" = +3.0V

3. Comparator reference supplies:

   "0" = +0.5V
   "1" = +2.5V

4. Window limits of programmed voltages: -0.1V to +7.0V

5. Window limits of programmed currents forced by PMU: -5mA to +5mA

Tester statements to implement the above could be written as follows:

Statement Number	Statement
1	SOCKET ID 0:
2	ENABLE VHI LT 7.0, RNG2;
3	ENABLE VLO GT -.1, RNG2;
4	ENABLE IHI LT 5E-3, RNG2;
5	ENABLE ILO GT -5E-3, RNG2;
6	ON TRIP, ABORT;
7	ENABLE TRIP1 GT 80E-3,RNG2;
10	FORCE VF1 5.0, RNG2;
11	MEASURE NODE 143;
12	IF VALUE LT 1E-3 THEN GO TO ABORT;
13	FORCE E1 3.0, RNG2;
14	FORCE E0 .5, RNG2;
15	SET S1 2.5, RNG2;
16	SET S0 0.5, RNG2;
17	ABORT: END;

The following is a brief analysis of the preceding tester statements:

S.N. 1 SOCKET ID O. This statement states that the load board identification code is 0. Execution of this statement causes the hardwired identifier code on the performance board to be compared with the code specified.

S.N. 2 & 3 The statements are used to specify the upper and lower limits against which all following programmed current/voltage statements are compared. The high limit is set to +7 volts and the low limit to -.1 volt.

S.N. 4 & 5 Statement numbers four and five satisfy the requirements of step five of the test parameters. The high and low current limits are set to +5 milliamps and -5 milliamps. Notice that current is written as 5E-3. The 5 merely states that it is 5 units of current, the E-3 represents 10^{-3} and places the decimal point three places to the left of the unit, i.e., .005 (5 milliamps). 5E-3 therefore is 5 milliamps. If the limit required was 5 microamps, the statement would be written as 5E-6 (.000005), 5 nanoamps would be written as 5E-9.

S.N. 6 This statement indicates that if the current from DPS1 exceeds the value specified in statement 7, transfer to the statement ABORT. ABORT can be the terminal END statement or it could be a section of the program intended to determine at what current level the device failed.

S.N. 7 The current trip device TRIP1, associated with VF1 is set to trip if power supply current flow exceeds 80 milliamps.

S.N. 10 This statement forces the VF1 (programmable voltage forcing supply) to 5.0 volts and sets the range to range 2.

S.N. 11 This statement causes a measurement of monitor point 143 in the tester which is DPT1.

S.N. 12 This statement aborts the test if the current drawn is less than 1 milliamp.

S.N. 13 & 14 These two statements set the voltage conditioners (E1 and E0 reference supplies) to specified values and ranges.

S.N. 15 & 16 These two statements set the comparator (S1 and S0 reference supplies) to specified values and ranges.

S.N. 17 This is the terminal END statement of the program.

In the example just completed, the test parameters were written out in five steps and were not included in the program. The test parameters and any other information could have been included as remarks. Any statement preceded by REM and terminated by a semicolon will cause no action by TOPSY, the statements are included for information purposes or as a reminder when examining a "source" program listing. e.g., REM EXPECTED VSAT IS 0.5 VOLTS, any statement preceded by the word WRITE with the statement enclosed in single quotes and terminated by a semicolon, will be executed by TOPSY, e.g., WRITE 'EXPECTED VSAT IS 0.5 VOLTS'; Executing this statement will cause EXPECTED VSAT IS 0.5 VOLTS to be dumped to the current output device. Similarly the computer can be informed that certain "noise words" exist in the program and should be ignored. "Noise words" are words intended to give a statement more English language readability.

Figure 4-1 shows an actual program which tests a Fairchild 9300 MSI circuit.

4.3.2 Functional Testing Statements

The various operations involved in performing functional testing usually include the following: define each tester pin connected to the device as an input or an output; establish each tester pin used as a "care" or "don't care" terminal; enable the comparators so that the comparison results of the test are stored for future use, such as data logging; apply a programmed input pattern to the device and compare the actual device outputs to programmed expected outputs. The user can also disable the comparators so that false failures are not indicated while interim test patterns are applied to set the device to a known state. In addition, the user can specify that the test program unconditionally branch to a specified tester statement number (or to the end of the program) if a failure occurs during functional testing.

Briefly, restated below are the functions of the various registers involved in function testing. Function testing is the application of logic levels ("1's" and "0's") to a digital device to ensure that it performs its designated functions according to a truth table.

Figure 4-2 is a simplified block diagram showing the basic circuitry associated with one pin. A minimum system consists of 30 pins worth of circuitry; additons to the system are made in groups of 30 pins up to a maximum of 120 pins. The driver and detector associated with each pin enables each pin to be considered as an input pin or an output pin, dependent upon programming of the registers.

```
000001    REM  9302 FUNCTIONAL AND PARAMETER TEST   SENTRY 400;
000001
000001    REM
000001
000001         TESTER PIN     DEVICE PIN     FUNCTION
000001
000001              1              19          CLOCK
000001              2              2           J
000001              3              3           K/
000001              4              4           P0
000001              5              5           P1
000001              6              6           P2
000001              7              7           P3
000001            DPS2             8           GROUND
000001              9              9           PE/
000001             10              1           MR
000001             11              11          Q3/
000001             12              12          Q3
000001             13              13          Q2
000001             14              14          Q1
000001             15              15          Q0
000001            DPS1             16          VCC;
000001
000001    FORCE VF2 0, RNG2;
000002    SET DELAY 1.5E-6;
000003    DCL VF/C,45/,IF1/-1.41E-3/,VCCMAX/5.25/,VCCMIN/4.75/;
000004    FORCE VF1 VCCMAX, RNG2;
000005              FORCE E0  .4, RNG2;
000006              FORCE E1 2.6, RNG2;
000007    FORCE FAR 0,4, RNG2;
000010    FORCE FA1 4.4, RNG2;
000011    GLOB1 = GLOB1 + 1;
000012    WRITE 'DEVICE ', GLOB1;
000013    ON TRIP, CHECK;
000014    ENABLE TRIP2 GT -0.937, RNG2;
000015    ENABLE TRIP1 GT 0.37, RNG2;
000016              SET S0  .5, RNG2;
000017              SET S1 2.5, RNG2;
000020                                        REM  PIN 1 IS CLOCK
000021                                             PIN 19 IS RESET;
000021              SET M 0000000000111111;
000022    SET S 1;
000023    DA FCT, ENDPMO;
000024    STRT:   REM   START OF LOOP;
000024              SET F 011111101010000;        REM  MASTER RESET;
000025              SET F 011111101110000;
000026              SET F 111111101110001;        REM  SERIAL IN 1;
000027    SET F 0;
000030              SET F 11111110111001;
000031    SET F 0;
000032              SET F 1111111011101;
000033    SET F 0;
000034              SET F 111111101101;
000035              SET F 00011101111;
000036              SET F 100111101101110;        REM  SERIAL IN 0;
000037    SET F 0;
000040              SET F 10011110110110;
000041    SET F 0;
000042              SET F 1001111011010;
000043    SET F 0;
000044              SET F 100111101110;
000045              SET F 01011110111;
000046              SET F 110111101110001;        REM  TOGGLE IN;
000047    SET F 0;
000050              SET F 110111101110010;
000051    SET F 0;
000052              SET F 110111101110101;
000053    SET F 0;
000054              SET F 110111101101010;
000055    SET F 0;
000056              SET F 110111101110101;
000057              SET F 00111110111;
000060              SET F 101111101101011;        REM  1ST CONST, OTHERS SHIFT;
000061              SET F 001010100011;     REM  PARALLEL IN;
000062              SET F 101010100010101;
000063              SET F 00110100001;
000064              SET F 101101001101011;
000065              SET F 111111101110101;        REM  ALL INPUTS HIGH FOR MIN
I;
000066    IF SWITCH EQ 1 THEN GOTO STRT;
000070    FORCE VF1 VCCMIN, RNG2;
000071    I=I+1;
000072    SET F (16) 1;              REM  PIN 16 INDICATES 2ND PASS;
000073    IF 1 EQ 1 THEN GOTO STRT;
000074
000075    REM  DC PARAMETER TESTS;
000075
000075    SET CLAMP POS 5.5;
000075    REM  INPUT LOW TESTS;
000076
000076        SET PMU SENSE,RNG2;
000077    SET PMU FORCEV, RNG2;
000100        FANIN=1;
000101    FORCE PMU 2.4;
000102    FOR PINN= 2 THRU 7 DO
000103          CALL IFTEST;
000104    PINN=10;  CALL IFTEST;
000105        PINN=9 ; FANIN=2,3; CALL IFTEST;
000111    PINN=11;  FANIN=4;  CALL IFTEST;
000114          XPMU PIN;
000115    DISABLE DCT0;
000116
000116          SUBR IFTEST;
000116          CPMU PIN PINN;
000117          FORCE VOLTAGE VF;
000120    ENABLE DCT0 LT IF1*FANIN;
000121          MEASURE VALUE;
000122    FORCE PMU 2.4;
000123    END;
000123
000123
000123    REM  INPUT LEAKAGE TESTS;
000123
000123    FORCE VF1 VCCMAX, RNG2;
000124    FORCE E1 4.5, RNG2;
000125    SET PMU SENSE, RNG1;
000126    FORCE PMU 4.5;
000127    SET DELAY 0,001, DC;
000130    ENABLE DCT1 GT ABE-6;
000131    FOR PIN = 2 THRU 7 DO CALL LEAK;
000133    PIN=13;  CALL LEAK;
000135    ENABLE DCT1 GT 2.3*60E-6;
000136    PIN=9;
000137    CALL LEAK;
000140    ENABLE DCT1 GT 4*60E-6;
000141    PIN=1;
000142    CALL LEAK;
000143    XPMU PIN;
000144    DISABLE DCT1;
000145
000145    SUBR LEAK;
000145    CPMU PIN PIN;
000146    FORCE DELAY;
000147    MEASURE VALUE;
000152    END;
000152
000152    REM  OUTPUT LOW VSAT TESTS;
000152
000150    SET F 011111101010000;        REM  MASTER RESET;
000151    ENABLE DCT0 GT 0,4;
000152    SET PMU SENSE, RNG1;
000153    SET PMU FORCEI, RNG2;
000154    TOL=9,4E-3;
000155    SET DELAY 2,5E-3, DC;
000156    FOR PIN=12 THRU 15 DO CALL LOAD;
000163    XPMU PIN;
000161    SET F 001111101110000;
000162    SET F 100111101011111;              REM  PIN 11 GOES LOW;
000163    PIN=11;
000164    CALL LOAD;
000165    XPMU PIN;
000166    DISABLE DCT0;
000167
000167    SUBR LOAD;
000167    CPMU PIN PIN;
000171    FORCE PMU 10U;
000171    MEASURE VALUE;
000172    FORCE PMU 0;
000173    END;
000173
000173
000173    REM  OUTPUT HIGH TESTS;
000173
000173    FORCE VF1 VCCMIN, RNG2;
000174    ENABLE DCT1 LT 2.4;
000175    TOL=0,25E-3;
000176    IOL=10M;
000177    SET PMU SENSE, RNG2;
000200    FOR PIN=12 THRU 15 DO CALL LOAD;
000202    XPMU PIN;
000203    SET F 011111101010000;          REM  PIN 11 GOES HIGH;
000204    PIN=11;
000205    CALL LOAD;
000206    XPMU PIN;
000207    GOTO ENDPMO;
000210
000210    CHECK:  REM  CURRENT TRIP TEST;
000217
000210    DISABLE DCT0;
000211    DISABLE DCT1;
000212    MEASURE MODE 143, LOG;
000213    X=VALUE;
000214    MEASURE MODE 144, LOG;
000215    WRITE 'IPC = ', X, '    IGND = ', VALUE;
000215
000216    ENDPMO:   FORCE RESET;
000217    END;
```

Figure 4-1. Actual Source Program Listing

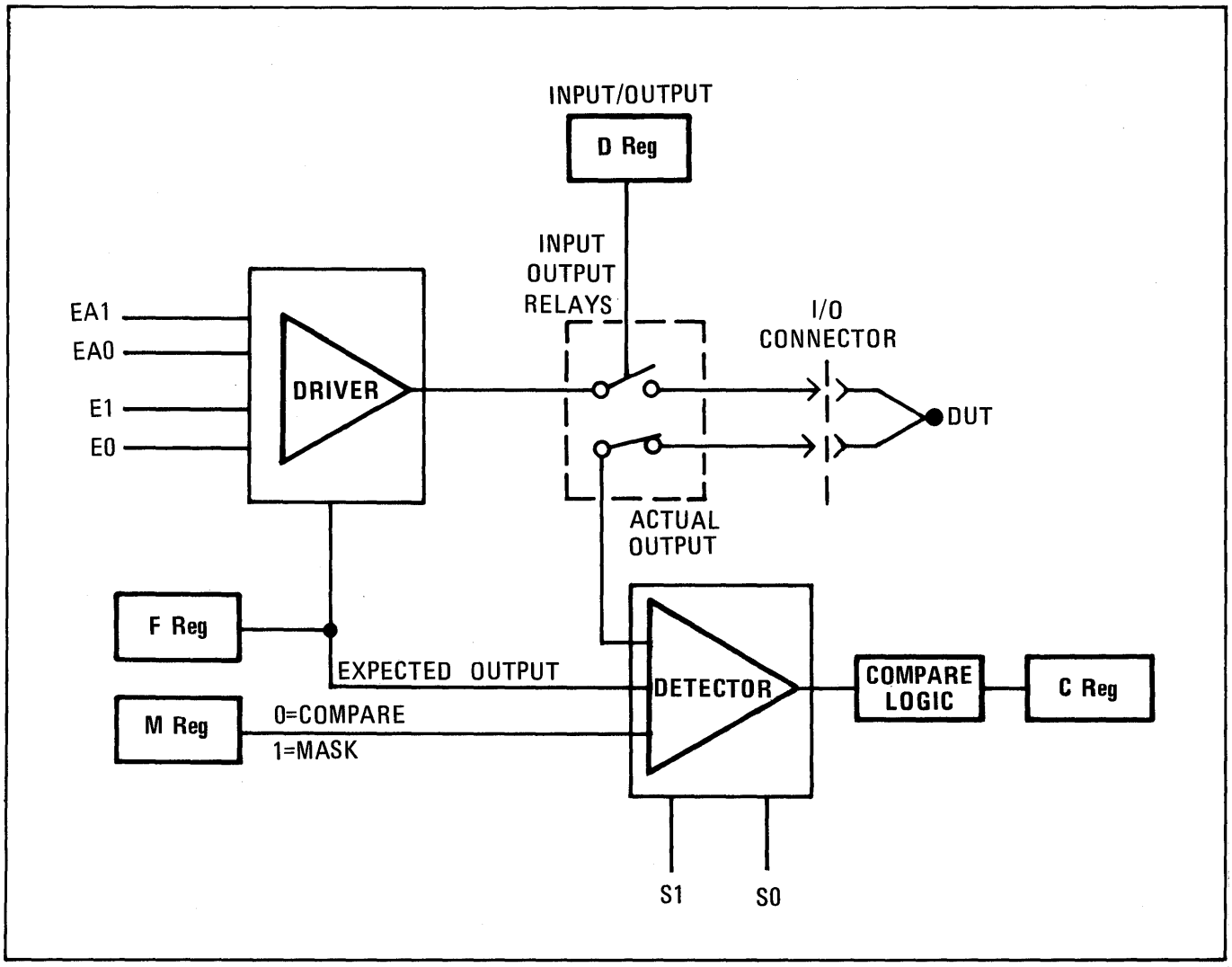

Figure 4-2. Simplified Block Diagram

The D register is termed the INPUT/OUTPUT register. If the D register is programmed as "1," the associated pin is defined as an input pin; consequently a relay is energized to connect the output of the driver to the pin. If the D register is programmed "0," the associated pin is defined as an output pin. The detector is always connected to the pin (except when the PMU is programmed to that pin) therefore, programming of the M register will determine whether the output of the detector is inhibited or enabled, to provide a pass/fail status for that pin.

The F register contains the logic patterns "0" or "1" to be applied to those pins defined as input pins by the D register. If the F register is programmed as a ("1") high level, the F register causes the high output of the driver to be applied to the associated pin. If the F register is programmed with a ("0") low level, the low output of the driver is applied to the pin. The F register also contains the expected logical output of those pins defined as output pins. The expected output is fed to the detector and compared with the actual output of the pin. If the inputs are equal, the detector will provide a "0" output that is interpreted as a pass condition. If no comparison exists, the detector will provide a "1" output that is interpreted as a fail condition.

The M register is the "care/don't care" or "mask" register. The output of the M register is applied as a third input to the detector. If the programmer is interested (care) in the pass/fail condition of a pin, the output of the M register is programmed as a "1." The care or "1" condition enables the detector to make the comparison between the actual voltage and the expected voltage. If the programmer is not interested (don't care) in the level of a pin, the M register is programmed as a "don't care" (Mask) or "0." The "don't care" condition inhibits the output of the detector. However, logic circuitry at the output of the detector will still provide a "0" level to the C register, and the function test fail output will indicate a pass. An input pin, or an output pin with an undefined state, would normally be programmed as "don't care" to prevent false failure indications on that pin.

Tester statements to accomplish function testing could be written as follows:

Statement Number	Statement
1	ON FCT, ABORT;
2	SET D 0 110 111 111;
3	SET M 0 001 000 000;
4	SET F 0 110 010 010;
5	SET F 0 011 000 000;
6	SET F 0 111 101 110;
7	SET F 0 100 100 100;
10	SET D 0 110 110 011;
11	SET M 0 000 001 100;
12	SET F 0 000 011 000;
13	SET F 0 000 000 110;
14	SET F 0 000 000 000;
15	DISABLE COMPARATORS;

The R register is the utility relay register and controls the utility relays (one per tester pin). A binary "1" indicates a closed relay and a binary "0" indicates an open relay. The utility relays may be used for such functions as connecting a load resistor to an output pin.

If the design of the device-under-test is such that more than one set of input patterns must be applied to set the DUT to a known state, a more efficient way to disable the comparators while the interim patterns are applied would be to use the ENABLE STROBE statement. To compare the efficiency of the two methods, first examine the following set of statements which use the ENABLE/DISABLE COMPARATOR statements:

Statement Number	Statement
1	ON TRIP, ABORT;
2	DISABLE COMPARATORS;
3	SET F 0 000 111 000;

Statement Number	Statement
4	ENABLE COMPARATORS;
5	SET F 1 000 111 000;
6	DISABLE COMPARATORS;
7	SET F 0 000 000 111;
10	ENABLE COMPARATORS;
11	SET F 1 000 000 111;
12	DISABLE COMPARATORS;
13	SET F 0 000 111 111;
14	ENABLE COMPARATORS;
15	SET F 1 000 111 111;

In the above example, test results are available to the user after executing statements 5, 11, and 15. Let us examine the same program again. This time, however, the ENABLE STROBE statement is used instead of the ENABLE/DISABLE COMPARATOR statements:

Statement Number	Statement
1	ON TRIPP, ABORT; DISABLE COMPARATORS;
2	ENABLE STROBE 1000;
3	SET F 0 000 111 000;
4	SET F 1 000 111 000;
5	SET F 0 000 000 111;
6	SET F 1 000 000 111;
7	SET F 0 000 111 111;
10	SET F 1 000 111 111;

In the above example, the same functional tests are executed as in the first example. Notice, however, that fewer program statements were required when using the ENABLE STROBE statement rather than the ENABLE/DISABLE COMPARATOR statements.

If programmed synchronous clocks are required for signal conditioning beyond the capabilities of the test head functional test patterns, one or any combination of four clock (or sync) pulses can be programmed to occur using the ENABLE CLOCK and SET CLOCK statements in conjunction with a series of SET F statements. As an example, assume a particular circuit on the DUT requires two successive clocks to cause the output state to go to a known condition. A sequence of statements to accomplish that requirement could be written as follows:

Statement Number	Statement
1	SET DELAY 350E-6;
2	ENABLE CLOCK 1000;
3	SET CLOCK 2;

Statement Number	Statement
4	ENABLE COMPARATORS;
5	SET F 1 000 000 000;
6	SET F 0 000 000 000;
7	SET F 1 000 000 111;

Figure 4-3 illustrates the timing sequence when executing statements 5, 6, and 7.

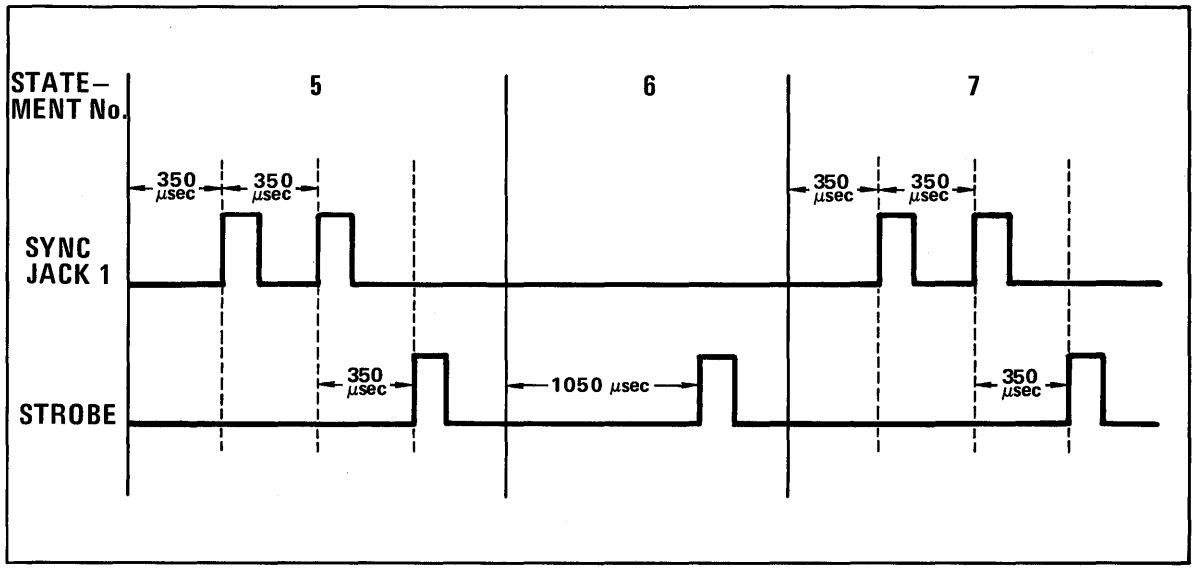

Figure 4-3. Programmed Clock Timing Examples

4.3.3 Program Simplification

When writing bit patterns into a register, the pattern can be programmed by specifying each bit of the pattern; the process is not too complicated if the device has 10 or 12 pins. However, if the device has 120 pins or 240 pins, which the system is quite capable of testing, the programmers task would be practically impossible. To simplify the process, the bit patterns can be modified by the use of two operators. The computer is programmed to recognize parenthesis (:) (Pattern replicator) and the bracket [ ] (pin origin statement) as modifiers to SET D, F, M, S, or R register instructions. Examine the two SET F instructions below:

1) SET F 0000 11 0000 11 000000000000000000000001;

2) SET F (4:0) 11 (4:0) 11 (23:0) 1;

In instruction No. 1, the bit pattern was laborously written out. Instruction No. 2 reads as follows. Set the first four bits to "0" followed by two "1's." Set the next four bits to "0" followed by two "1's." Set the next 23 bits to "0" followed by one 1. The two statements are identical.

Examine the two SET F instructions below:

1) SET F 01010101 11 01010101 11111 00 11111111 0101 1;

2) SET F (4:01) 11 (4:01) (5:1) 00 (8:1) (2:01) 1;

Again the bit pattern was laboriously written out. Instruction No. 2 reads as follows: Insert four groups of 01, followed by two "1's," followed by four groups of 01, followed by five "1's," followed by two "0's," followed by eight "1's," followed by two groups of 01, followed by 1. We could just as easily write 120 bits alternating with "1's" and "0's" as (60:10); another configuration could be (12:10001); i.e., the number of bits within the parenthesis (pattern replicator) after the colon are repeated successively by the number before the colon. The pattern replicator is therefore used to reduce the number of "1's" and "0's" contained within a SET D, F, M, S, or R register instruction. The brackets [ ] (pin origin) indicate the starting pin number to be affected by the following bit or bit pattern when contained within any SET D, F, M, S, or R register instruction. Examine the four statements below.

1) SET F 0000 11 0000 11 0000 111100;

2) SET F (4:0) 11 (4:00) 11 (4:0) (5:0) 00;

3) SET F [6] 01;

4) SET F [2] 11 [7] 11 [11] 00;

The first two statements are quite straight forward. In the third statement, starting with bit [6], bit 6 is changed to 0 and bit 7 to 1, all other bits remain the same. In the fourth statement starting with bit [2] bits 2 and 3 are changed to "1's," starting with bit [7] bits 7 and 8 are changed to "1's," starting with bit [11] bits 11 and 12 are changed to "0's," all other bits remain the same. It is not necessary to initially program a register with "1's" and "0's" before either the pattern replicator or pin origin modifiers can be used. It is assumed that all registers are set to "0's" before the program is started (either through a computer RESET or manual RESET), therefore, all changes are made to the zero status, subsequent changes are made to the preceding status, and all nonaddress pins will take on previously specified values.

NOTE

The compiler only generates patterns for the ranks in which pin changes occur. If a conditional branch is used, the registers must be redefined when entering the loop.

4.3.4 DC Testing Statements

Two types of DC tests can be programmed using the Sentry 400 Tester Statements; they are: Force a voltage on pin "n" and measure the current or force a current and measure the voltage. The following paragraphs describe different methods by which these operations can be implemented.

FORCE VOLTAGE/MEASURE CURRENT: This operation can be programmed by one of two methods. If the measurement is to be made for one value of forcing voltage only, the statements could be written as follows:

Statement Number	Statement
1	SET PMU SENSE, RNG2;
2	FORCE VOLTAGE .45, RNG2;
3	MEASURE VALUE;

If a measurement is to be made for more than one value of forcing voltage, in the same range, the statements could be written as follows:

Statement Number	Statement
1	SET PMU SENSE, RNG2;
2	SET PMU FORCEV, RNG2;
3	FORCE PMU .45;
4	MEASURE VALUE;
5	FORCE PMU 4.0;
6	MEASURE VALUE;
7	FORCE PMU 4.5;
10	MEASURE VALUE;

FORCE CURRENT/MEASURE VOLTAGE: Programming this operation is similar to that of the FORCE VOLTAGE/MEASURE CURRENT type: the only difference being the substitution of VOLTAGE for CURRENT, and CURRENT for VOLTAGE in the statements. A single measurement could be written:

Statement Number	Statement
1	SET PMU SENSE, RNG2;
2	FORCE CURRENT -180E-6, RNG1;
3	MEASURE VALUE;

For more than one value of forcing current, in the same range, the statements could be written:

Statement Number	Statement
1	SET PMU SENSE, RNG2;
2	SET PMU FORCEI, RNG1;
3	FORCE PMU -180E-6;
4	MEASURE VALUE;
5	FORCE PMU -20E-6;
6	MEASURE VALUE;

MEASURE VOLTAGE/NO CURRENT FLOW: To make a voltage measurement only (i.e., with no loading or infinite impedance) the PMU must be programmed to force zero current; this could be accomplished as follows:

Statement Number	Statement
1	SET PMU SENSE, AUTO;
2	FORCE CURRENT 0, RNG0;
3	MEASURE VALUE;

4.3.5 Programming Rules

As in any computer controlled system there are certain rules to be followed if correct and efficient programming is to be achieved.

1. A FACTOR language program consists of abbreviated English language statements. The majority of these statements are contained in Table 4-1 and are supplemented by the FACTOR Manual.

2. Noise words, are words that the programmer may use to give the abbreviated statements more readibility. The words must be listed in a statement, e.g.,

   NOISE VOLTS, AMPS, SECS;

3. Remarks may be inserted throughout the program. Any statement preceded by REM and terminated by a semicolon will cause no action by TOPSY. The statement will be printed on the source program listing.

4. Any text (except quote marks) preceded by the word WRITE, enclosed in single quotes and terminated by a semicolon will be dumped to the output device. No test station action occurs.

5. The REM statement may be listed by separate sequence number, or they may be included on the same line of a statement to which the remark refers.

6. All statements must be terminated by a semicolon.

7. FACTOR accommodates: numbers as integers, decimal fractions and exponentials; handles Boolean and scalar variables; arrays (ordered series of variables); parametered calls; and a wide variety of other functions, as specified in the FACTOR Manual.

8. Subroutines and Functions can be used to avoid rewriting the same statements at various points in a program. Blocks are used to establish a LOCAL context for the variables and labels defined therein.

```
BLOCK (a)
 BLOCK (b)
 END (b)
 BLOCK (c)
  BLOCK (d)
  END (d)
 END (c)
END (a)
```

Any number of subroutines can be placed in up to eight nesting levels, and subroutines can be called as often as desired. The global variables are quantities accessible to all blocks.

9. Various statements such as IF, THEN, GOTO, and so on, may be used to mix and match sequences of instructions and branches, in response to test results. For instance, IF an element fails a critical test, GOTO an analysis routine to find out why, and THEN put the element into the reject bin.

4.3.6 Device Program Preparation

The initial step in preparing a device program is usually a handwritten list of FACTOR commands comprising the program.

A FACTOR language program consists of abbreviated English language statements. Each statement is a command to carry out some action. When the user program is executed, these commands are carried out sequentially in the order written. There are, however, commands to change this sequential execution and cause it to begin again at a specified statement, quite possibly one other than the next sequential statement after the one last executed. Because this transfer of control is possible FACTOR needs a definite way to indicate where each statement ends. Consequently, every statement must be followed by a semicolon, the word END or the word ELSE. The word END is used at the end of a program or subroutine. The word ELSE is used when a choice is involved and the semicolon is used to terminate a statement in a series of statements. Of the three, the semicolon is the most common.

The statement is the basic unit of a compiler language program. Examine the Sentry 400 FACTOR coding form.

Statements and labels can occupy any of the first 72 characters of an input record (card, MT, TTY). The last 8 characters of each record are reserved for sequence numbers. Several statements can appear on a record, as space permits, or a single statement can be strung over several records. In any case there is one sequence number per record even if the remainder of record is blank. It is suggested however, that column 65 should not be exceeded so listings with statement numbers will fit on the 80 column teletype or line printer without continuation lines.

The recommended method as shown in the coding form is to use the first eight columns for the LABEL, the ninth column for a colon (:), the tenth column is a blank. The command is started in the eleventh column and terminated by a semicolon.

The programmer may or may not assign sequence numbers at his option since the compiler will not flag blank sequence fields as sequence errors.

Labels, variables, arrays, subroutines, and functions must be named by a legal identifier consisting of up to 8 alphanumeric characters, the first an alpha.

On the example coding form, several hand written statements are shown (the complete program–369_{10} statements–is not shown). The statements were then transferred onto punched cards (one statement per card in this case). The punched cards were then fed into a card reader and transferred to the computer. On typing // COMPILE '* SAN1' LIST the following listing was produced on the TTY. This test program should serve to illustrate how the Sentry 400 Tester Statements were utilized to perform functional, as well as DC parameter testing on an actual device. As a matter of interest, DOPSY took 33 seconds to compile this program.

Statement 1 contains two remarks defining the following tests as function, parameter and probe test sequences. The probe test sequence contains a statement to unconditionally branch to the location MSSAGE (Statement No. 001227) if a function test failure occurs.

000025_8

This statement defines that the device uses negative true logic and sets the delay to 50 microseconds.

000035_8 –000472_8

This is a group of SET F statements. The various combinations were developed by a computer and hence each bit was printed out. This group illustrates quite clearly the usefulness of the pattern replicator (:) and pin origin [ ] operators to a programmer.

These statements each call on the subroutine labeled NLEAK (Statement No. 00152) and performs that subroutine on each specified pin. Further on in the program, subroutines labeled, ZLEAK, YLEAK, and WLEAK, etc., are called upon to perform tests on specified pins. Each of these subroutines call for the PMU to force a voltage and measure the leakage current through a specified pin. After the completion of each subroutine or statement, the tester moves to the next statement and continues on to the end of the program.

FAIRCHILD
SYSTEMS TECHNOLOGY

SENTRY 400 FACTOR CODING FORM

PROGRAMMER: JOHN DOE | DATE: 6/7/70 | PROGRAM: '* SAN' | PAGE 1 OF XX

```
LABEL :   COMMAND                                                          SEQUENCE NUMBER
1     6 7 9   15   20   25   30   35   40   45   50   55   60   65   70 72   75   80
REM SENTRY 400 FUNCTION AND PARAMETER TEST SEQUENCE FOR 'SA';

REM PROBE TEST SEQUENCE;
ON FCT, MSSAGE;
SET SØ -2, RNG2;
SET M ID (16:7) D (17:1);
SET DELAY 20E-3, DC;
SET PMU FORCEV, RNG2;
SET PMU SENSE, RNG1;
CPMU PIN 2;
FORCE PMU -5;
SET F Ø;
FORCE PMU Ø;
XPMU PIN;
```

Figure 4-4. Sentry 400 Factor Coding Form

```
//.COMPILE '*SAN1' LIST
000001      REM  SENTRY 400 FUNCTION AND PARAMETER TEST SEQUENCE FOR 'S
000001
000001      REM  PROBE TEST SEQUENCE;
000001      ON FCT, MSSAGE;
000002      SET S0 -2, RNG2;
000003      SET M 10 (16:1) 0 (17:1);
000004      SET DELAY 20E-3, DC;
000005      SET PMU FORCEV, RNG2;
000006      SET PMU SENSE, RNG1;
000007      CPMU PIN 2;
000010      FORCE PMU -5;
000011      SET F 0;
000012      FORCE PMU 0;
000013      XPMU PIN;
000014
000014      REM  FUNCTION TEST SEQUENCE;
000014
000014      ON FCT,ABORT;
000015      FORCE VF2 0,RNG2;
000016      FORCE VF1 -7.0,RNG2;
000017      FORCE E0 0.0; FORCE E1 -7.0;
000021      FORCE EA0 -20.0,RNG3;
000022      FORCE EA1 -20.0,RNG3;
000023      SET S0 -1.5; SET S1 -4.0;
000025      SET LOGIC NEG; SET DELAY 50E-6;
000027      SET R [2] 101 [7] 111 [16] 1;
000030      SET S [1] 1 [12] 1;
000031      SET D 10101100011110001101111111111111110010;
000032      SET M (36:1);
000033      SET M 00 [12] 0 [19] 0 [36] 0;
000034      FORCE DELAY;
000035      SET F 0101100100011111001000000000000000011;
000036      SET F 0101100100011111001000000000000000011;
000037      SET F 0101100100010111001000000000000000011;
000040      SET F 0101110101111111001000000000000001001;
000041      SET F 0101110101111011001000000000000001001;
000042      SET F 0101110101111111001000000000000001001;
000043      SET F 0101110101111011001000000000000001001;
000044      SET F 0101110101111111001000000000000001001;
000045      SET F 0101110101111011001000000000000001001;
000046      SET F 0101110101111111001000000000000001001;
000047      SET F 0101110101111011001000000000000001001;
000050      SET F 0101110101111111001000000000000001001;
000051      SET F 0101110101111011001000000000000001001;
000052      SET F 0101110101111111001000000000000001001;
000053      SET F 0101110101111011001000000000000001001;
000054      SET F 0101110101111111001000000000000001001;
000055      SET F 0101110101111011001000000000000001001;
000056      SET F 0101110101111111001000000000000001001;
000057      SET F 0101110101111011001000000000000001001;
000060      SET F 0101110101111111001000000000000001001;
000061      SET F 0101110101111011001000000000000001001;
000062      SET F 0101110101111111001000000000000001001;
000063      SET F 0101110101111011001000000000000001001;
```

Figure 4-5. Sentry 400 Device Program

```
000064      SET F 0101110101111111001000000000000001001;
000065      SET F 0101110101111011100100000000000001001;
000066      SET F 0101110101111111100100000000000001001;
000067      SET F 0101110101111011100100000000000001001;
000070      SET F 0101110101111111100100000000000001001;
000071      SET F 0101110101111011100100000000000001001;
000072      SET F 0101110101111111100100000000000001001;
000073      SET F 0101110101111011100100000000000001001;
000074      SET F 0101110101111111100100000000000001001;
000075      SET F 0101110101111011100100000000000001001;
000076      SET F 0101110101111111100100000000000001001;
000077      SET F 0101110101111011100100000000000001001;
000100      SET F 0101110101111111100100000000000001001;
000101      SET F 0101110101111011100100000000000001001;
000102      SET F 0101110101111111100100000000000001001;
000103      SET F 0101110101111011100100000000000001001;
000104      SET F 0101110101111111100100000000000001001;
000105      SET F 0101110101111011100100000000000001001;
000106      SET F 0101110101111111100100000000000001001;
000107      SET F 0101110101111011100100000000000001001;
000110      SET F 0101110101111111100100000000000001001;
000111      SET F 0101110101111011100100000000000001001;
000112      SET F 0101110101111111100100000000000001001;
000113      SET F 0101110101111011100100000000000001001;
000114      SET F 0101110101111111100100000000000001001;
000115      SET F 0101110101111011100100000000000001001;
000116      SET F 0101110101111111100100000000000001001;
000117      SET F 0101110101111011100100000000000001001;
000120      SET F 0101110101111111100100000000000001001;
000121      SET F 0101110101111011100100000000000001001;
000122      SET F 0101110101111111100100000000000001001;
000123      SET F 0101110101111011100100000000000001001;
000124      SET F 0101110101111111100100000000000001001;
000125      SET F 0101110101111011100100000000000001001;
000126      SET F 0101110101111111100100000000000001001;
000127      SET F 0101110101111011100100000000000001001;
000130      SET F 0101110101111111100100000000000001001;
000131      SET F 0101110101111011100100000000000001001;
000132      SET F 0101110101111111100100000000000001001;
000133      SET F 0101110101111011100100000000000001001;
000134      SET F 0101110101111111100100000000000001001;
000135      SET F 0101110101111011100100000000000001001;
000136      SET F 0101110101111111100100000000000001001;
000137      SET F 0101110101111011100100000000000001101;
000140      SET F 0101110101111111100100000000000001101;
000141      SET F 0101110101111011100100000000000001101;
000142      SET F 0101110101111111100100000000000001101;
000143      SET F 0100110101111011100100000000000001101;
000144      SET F 0100110101111111100100000000000001101;
000145      SET F 0100110101111011100100000000000001101;
000146      L1:  SET D 1010110001111000110111111111111111110;
000147      SET M 0001001110000111000000000000000000000;
000150      SET F 0100110101111011111111111111111111101;
000151      SET F 0100110101111011111111111111111111001;
```

Figure 4-5. (Cont.)

```
000152      SET F 0100110101110111111111111111111111101;
000153      SET F 0100110101110111111111111111111111001;
000154      SET F 0100110101110111111111111111111111101;
000155      SET F 0100110101110111111111111111111111001;
000156      SET F 0100110101110111111111111111111111101;
000157      SET F 0100110101110111111111111111111111001;
000160      SET F 0100110101110111111111111111111111101;
000161      SET F 0100110101110111111111111111111111001;
000162      SET F 0100110101110111111111111111111111101;
000163      SET F 0100110101110111111111111111111111001;
000164      SET F 0100110101110111111111111111111111101;
000165      SET F 0100110101110111111111111111111111001;
000166      SET F 0100110101110111111111111111111111101;
000167      SET F 0100110101110110111111111111111111001;
000170      SET F 0100110101110110111111111111111111101;
000171      SET F 0100110101110111111111111111111111001;
000172      SET F 0100110101110111111111111111111111101;
000173      SET F 0100110101110111111111111111111111001;
000174      SET F 0100110101110111111111111111111111101;
000175      SET F 0100110101110111111111111111111111001;
000176      SET F 0100110101110111111111111111111111101;
000177      SET F 0100110101110111111111111111111111001;
000200      SET F 0100110101110111111111111111111111101;
000201      SET F 0100110101110111111111111111111111001;
000202      SET F 0100110101110111111111111111111111101;
000203      SET F 0100110101110111111111111111111111001;
000204      SET F 0100110101110111111111111111111111101;
000205      SET F 0100110101110111111111111111111111001;
000206      SET F 0100110101110111111111111111111111101;
000207      SET F 0100110101110111111111111111111111001;
000210      SET F 0100110101110111111111111111111111101;
000211      SET F 0100110101110111111111111111111111001;
000212      SET F 0100110101110111111111111111111111101;
000213      SET F 0100110101110101111111111111111111001;
000214      SET F 0100110101110101111111111111111111101;
000215      SET F 0100110101110111111111111111111111001;
000216      SET F 0100110101110111111111111111111111101;
000217      SET F 0100110101110111111111111111111111001;
000220      SET F 0100110101110111111111111111111111101;
000221      SET F 0100110101110111111111111111111111001;
000222      SET F 0100110101110111111111111111111111101;
000223      SET F 0100110101110111111111111111111111001;
000224      SET F 0100110101110111111111111111111111101;
000225      SET F 0100110101110111111111111111111111001;
000226      SET F 0100110101110111111111111111111111101;
000227      SET F 0100110101110011111111111111111111001;
000230      SET F 0100110101110011111111111111111111101;
000231      SET F 0100110101110011111111111111111111001;
000232      SET F 0100110101110011111111111111111111101;
000233      SET F 0100110101110011111111111111111111001;
000234      SET F 0100110101110011111111111111111111101;
000235      SET F 0100110101110011111111111111111111001;
000236      SET F 0100110101110011111111111111111111101;
000237      SET F 0100110101110011111111111111111111001;
```

Figure 4-5. (Cont.)

```
000240      SET F 0100110101111001111111111111111111111101;
000241      SET F 0100110101111001111111111111111111111001;
000242      SET F 0100110101111001111111111111111111111101;
000243      SET F 0100110101111001111111111111111111111001;
000244      SET F 0100110101111001111111111111111111111101;
000245      SET F 0100110101111001111111111111111111111001;
000246      SET F 0100110101111001111111111111111111111101;
000247      SET F 0100110101111011111111111111111111111001;
000250      SET F 0100110101111011110010000000000000000001;
000251      SET F 0100110101111011110010000000000000000101;
000252      SET F 0100110101111011110010000000000000000001;
000253      SET F 0100110101111011110010000000000000000101;
000254      SET F 0100110101111011110010000000000000000001;
000255      SET F 0100110101111011110010000000000000000101;
000256      SET F 0100110101111011110010000000000000000001;
000257      SET F 0100110101111011110010000000000000000101;
000260      SET F 0100110101111011110010000000000000000001;
000261      SET F 0100110101111011110010000000000000000101;
000262      SET F 0100110101111011110010000000000000000001;
000263      SET F 0100110101111011110010000000000000000101;
000264      SET F 0100110101111011110010000000000000000001;
000265      SET F 0100110101111011110010000000000000000101;
000266      SET F 0100110101111011110010000000000000000001;
000267      SET F 0100110101111011110010000000000000000101;
000270      SET F 0100110101111011000100000000000000000001;
000271      SET F 0100110101111011000100000000000000000101;
000272      SET F 0100110101111011000100000000000000000001;
000273      SET F 0100110101111011000100000000000000000101;
000274      SET F 0100110101111011000100000000000000000001;
000275      SET F 0100110101111011000100000000000000000101;
000276      SET F 0100110101111011000100000000000000000001;
000277      SET F 0100110101111011000100000000000000000101;
000300      SET F 0100110101111011000100000000000000000001;
000301      SET F 0100110101111011000100000000000000000101;
000302      SET F 0100110101111011000100000000000000000001;
000303      SET F 0100110101111011000100000000000000000101;
000304      SET F 0100110101111011000100000000000000000001;
000305      SET F 0100110101111011000100000000000000000101;
000306      SET F 0100110101111011000100000000000000000001;
000307      SET F 0100110101111011000100000000000000000101;
000310      SET F 0100110101111011000100000000000000000001;
000311      SET F 0100110101111011000100000000000000000101;
000312      SET F 0100110101111011000100000000000000000001;
000313      SET F 0100110101111011000100000000000000000101;
000314      SET F 0100110101111011000100000000000000000001;
000315      SET F 0100110101111011000100000000000000000101;
000316      SET F 0100110101111011000100000000000000000001;
000317      SET F 0100110101111011000100000000000000000101;
000320      SET F 0100110101111011000100000000000000000001;
000321      SET F 0100110101111011000100000000000000000101;
000322      SET F 0100110101111011000100000000000000000001;
000323      SET F 0100110101111011000100000000000000000101;
000324      SET F 0100110101111011000100000000000000000001;
000325      SET F 0100110101111011000100000000000000000101;
```

Figure 4-5. (Cont.)

```
000326      SET F 0100110101111011000100000000000000001;
000327      SET F 0100110101111011000100000000000000101;
000330      SET F 0100110101111001100100000000000000001;
000331      SET F 0100110101111001100100000000000000101;
000332      SET F 0100110101111001100100000000000000001;
000333      SET F 0100110101111001100100000000000000101;
000334      SET F 0100110101111001100100000000000000001;
000335      SET F 0100110101111001100100000000000000101;
000336      SET F 0100110101111001100100000000000000001;
000337      SET F 0100110101111001100100000000000000101;
000340      SET F 0100110101111001100100000000000000001;
000341      SET F 0100110101111001100100000000000000101;
000342      SET F 0100110101111001100100000000000000001;
000343      SET F 0100110101111001100100000000000000101;
000344      SET F 0100110101111001100100000000000000001;
000345      SET F 0100110101111001100100000000000000101;
000346      SET F 0100110101111001100100000000000000001;
000347      SET F 0100110101111001100100000000000000101;
000350      SET F 0100110101111011100100000000000000001;
000351      SET F 0101100100011111100100000000000000011;
000352      SET F 0101100100010111100100000000000000011;
000353      SET F 0111110101111111100100000000000000001;
000354      SET F 0111110101111011100100000000000000001;
000355      SET F 0111110101111111100100000000000000001;
000356      SET F 0111110101111011100100000000000000001;
000357      SET F 0111110101111111100100000000000000001;
000360      SET F 0111110101111011100100000000000000001;
000361      SET F 0111110101111111100100000000000000001;
000362      SET F 0111110101111011100100000000000000001;
000363      SET F 0111110101111111100100000000000000001;
000364      SET F 0111110101111011100100000000000000001;
000365      SET F 0111110101111111100100000000000000001;
000366      SET F 0101110101111111100100000000000000001;
000367      SET F 0101110101111111100100000000000000101;
000370      SET F 0100110101111011100100000000000000101;
000371      SET F 0100110101111111100100000000000000101;
000372      SET F 0100110101111011100100000000000000101;
000373      SET F 0100110101111111100100000000000000101;
000374      SET F 0100110101111011100100000000000000101;
000375      SET F 0100110101111111100100000000000000101;
000376      SET F 0100110101111011100100000000000000101;
000377      SET F 0100110101111011100100000000000000001;
000400      SET F 0100110101111011100100000000000000101;
000401      SET F 0100110101111011100100000000000000001;
000402      SET F 0100110101111011100100000000000000101;
000403      SET F 0100110101111011100100000000000000001;
000404      SET F 0100110101111011100100000000000000101;
000405      SET F 0100110101111011100100000000000000001;
000406      SET F 0100110101111011100100000000000000101;
000407      SET F 0100110101111011100100000000000000001;
000410      SET F 0100110101111011100100000000000000101;
000411      SET F 0100110101111011100100000000000000001;
000412      SET F 0100110101111011100100000000000000101;
000413      SET F 0100110101111011100100000000000000001;
```

Figure 4-5. (Cont.)

```
000414      SET F 0100110101110111001000000000000000101;
000415      SET F 0100110101110110001000000000000000001;
000416      SET F 0100110101111111001000000000000000001;
000417      SET F 0100110101111111001000000000000000101;
000420      SET F 0101110101110110001000000000000000101;
000421      SET F 0101110101111111001000000000000000101;
000422      SET F 0101110101110110001000000000000000101;
000423      SET F 0101110101111111001000000000000000101;
000424      SET F 0101110101110110001000000000000000101;
000425      SET F 0101110101110110001000000000000000001;
000426      SET F 0101110101111111001000000000000000001;
000427      SET F 0101110101110110001000000000000000001;
000430      SET F 0101110101111111001000000000000000001;
000431      SET F 0100110101110110001000000000000000001;
000432      SET F 0100110101110110001000000000000000101;
000433      SET F 0100110101110110001000000000000000001;
000434      SET F 0100110101110110001000000000000000101;
000435      SET F 0100110101110110001000000000000000001;
000436      SET F 0100110101110110001000000000000000101;
000437      SET F 0100110101110110001000000000000000001;
000440      SET F 0100110101110110001000000000000000101;
000441      SET F 0100110101110110001000000000000000001;
000442      SET F 0100110101110110001000000000000000101;
000443      SET F 0100110101110110001000000000000000001;
000444      SET F 0100110101110110001000000000000000101;
000445      SET F 0100110101110110001000000000000000001;
000446      SET F 0100110101110110001000000000000000101;
000447      SET F 0100110101110110001000000000000000001;
000450      SET F 0100110101110110001000000000000000101;
000451      SET F 0100110101110110001000000000000000001;
000452      SET F 0100110101110110001000000000000000101;
000453      SET F 0100110101110110001000000000000000001;
000454      SET F 0101101011111011100100000000000001001;
000455      SET F 0101101011111011000100000000000000001;
000456      SET F 0101101011010110001000000000000000001;
000457      SET F 0100110101010110001000000000000000001;
000460      SET F 0101111011110111001000000000000001001;
000461      SET F 0101111011110110001000000000000000001;
000462      SET F 0100110101010110001000000000000000001;
000463      SET F 0101011001010111001000000000000001001;
000464      SET F 0101011001010110001000000000000000001;
000465      SET F 0100110101010110001000000000000000001;
000466      SET F 0101111011110111001000000000000001001;
000467      SET F 0101111011110110001000000000000000001;
000470      SET F 0100110100110110001000000000000000001;
000471      SET F 0101100010001111100100000000000000011;
000472      SET F 0101100010001011100100000000000000011;
000473      SET D (60:0); SET M (60:0); SET R (35:0);
000476
000476      REM  PARAMETER TEST SEQUENCE;
000476
000476      DCL LEAKAGE,VF,IFC,VOLTS,IPIN,VOLTS1,VOLTS2,LEAK1,LEAK2;
000477      SET D (18:1)0(17:1);
000500      FORCE E1 -20.0;
```

Figure 4-5. (Cont.)

```
000501      FORCE E0 0;
000502      SET F (37:0);
000503      SET S (37:0);
000504      VF=-6.3;
000505      LEAKAGE =-100E-9;
000506      IPIN=17; CALL NLEAK;
000510      IPIN=18; CALL NLEAK;
000512      IPIN=22; CALL NLEAK;
000514      IPIN=23; CALL NLEAK;
000516      IPIN=24; CALL NLEAK;
000520      IPIN=25; CALL NLEAK;
000522      IPIN=26; CALL NLEAK;
000524      LEAKAGE=-500E-9;
000525      IPIN=27; CALL NLEAK;
000527      IPIN=28; CALL NLEAK;
000531      IPIN=29; CALL NLEAK;
000533      IPIN=30; CALL NLEAK;
000535      IPIN=31; CALL NLEAK;
000537      IPIN=32; CALL NLEAK;
000541      IPIN=33; CALL NLEAK;
000543      IPIN=35; CALL NLEAK;
000545      IPIN=3 ; CALL NLEAK;
000547      IPIN=5 ; CALL NLEAK;
000551      IPIN=6 ; CALL NLEAK;
000553      IPIN=10; CALL NLEAK;
000555      IPIN=11; CALL NLEAK;
000557      IPIN=13; CALL NLEAK;
000561      IPIN=21; CALL NLEAK;
000563      SET D 11(9:0)1(23:0)1;
000564      SET F 1(10:0)1(24:0);
000565      IPIN=7; CALL NLEAK;
000567      IPIN=8; CALL NLEAK;
000571      IPIN=9 ; CALL NLEAK;
000573      FORCE EA1 -6.3;
000574      FORCE EA0 0;
000575      SET D [35]1;
000576      SET S [35]1;
000577      SET F [35]1;
000600      IPIN= 16; CALL NLEAK;
000602      SET D (18:1)0(17:1);
000603      SET S (37:0);
000604      SET F (37:0);
000605      LEAKAGE = -100E-9;
000606      IPIN=20; CALL NLEAK;
000610      FORCE E1 -11.8;
000611      FORCE EA1 -6.3;
000612      FORCE EA0 0;
000613      SET S (34:0) 10;
000614      SET F 1(10:0)1(22:0)10;
000615      LEAKAGE=-500E-9;
000616      IPIN=4;CALL NLEAK;
000620      SET D 11(9:0)1(22:0)11;
000621      SET S (34:0)11;
000622      SET F 1(10:0)1(22:0)11;
```

Figure 4-5. (Cont.)

```
000623      IFC=0;
000624      VOLTS=-6.05;
000625      IPIN=14; CALL THRESHMIN;
000627      SET D [33]1[35]0;
000630      SET S [33]1;
000631      SET F [33]1;
000632      IPIN=15; CALL THRESHMIN;
000634      SET D 110011(3:0)(3:1)(23:0)1;
000635      SET S (4:0)11(4:0)1(24:0)1;
000636      SET F (4:0)11(4:0)11(23:0)1;
000637      LEAKAGE=-120E-6;
000640      VF=-6.3;
000641      IPIN=36; CALL ZLEAK;
000643      SET D [13]1[35]1;
000644      SET S [13]1[35]1;
000645      SET F [1]1[13]1[35]1;
000646      LEAKAGE=-1.5E-3;
000647      VF=-6.3;
000650      IPIN=36; CALL YLEAK;
000652      SET D 11(33:0)1;
000653      SET S (35:0)1;
000654      SET F (35:0)1;
000655      LEAKAGE=-100E-9;
000656      VF=-11.8;
000657      IPIN=12; CALL NLEAK;
000661      LEAKAGE=-1.0E-3;
000662      VF=-11.8;
000663      IPIN=1; CALL ZLEAK;
000665      SET D 11(9:0)1(23:0)1;
000666      SET S (35:0)1;
000667      SET F (11:0) 1 (23:0) 1;
000670      LEAK1=29.0E-6;LEAK2=11.0E-6;
000672      VF=-0.8;
000673      IPIN=35; CALL WLEAK;
000675      IPIN=5; CALL WLEAK;
000677      IPIN=6; CALL WLEAK;
000701      IPIN=10;  CALL WLEAK;
000703      SET F [1]1;
000704      IPIN=11; CALL WLEAK;
000706      IPIN=31; CALL WLEAK;
000710      IPIN=32; CALL WLEAK;
000712      IPIN=20; CALL WLEAK;
000714      IPIN=21; CALL WLEAK;
000716      IPIN=27; CALL WLEAK;
000720      IPIN=28; CALL WLEAK;
000722      IPIN=29; CALL WLEAK;
000724      IPIN=30; CALL WLEAK;
000726      IPIN=3 ; CALL WLEAK;
000730      LEAK1=60.0E-6; LEAK2=22.0E-6;
000732      IPIN=13; CALL WLEAK;
000734      IPIN=33; CALL WLEAK;
000736      LEAK1=80.0E-6; LEAK2=35.0E-6;
000740      SET D [35]1;
000741      SET S [35]1;
```

Figure 4-5. (Cont.)

```
000742      SET F [35]1;
000743      IPIN=14; CALL WLEAK;
000745      IPIN=15; CALL WLEAK;
000747      SET D 11001(4:0)101(4:0)110(13:1)0011;
000750      SET S (4:0)1(29:0)11;
000751      SET F 1(3:0)1(6:0)1(22:0)11;
000752      VOLTS1=-0.15; VOLTS2=-0.7;
000754      IFC=-100E-6;
000755      IPIN=7; CALL WTHRESH;
000757      IPIN =9; CALL WTHRESH;
000761      FORCE E1 -6.3;
000762      FORCE EA1 -11.8;
000763      FORCE E0 0;
000764      FORCE EA0 0;
000765      SET D (3:1)0(2:1)(3:0)(4:1)(3:0)(2:1)0(14:1)011;
000766      SET S 1(10:0)1(24:0);
000767      SET F 10101(4:0)(4:1)(19:0)1001;
000770      SET F [13]0,[13]1,[13]0,
000774      [13]1,[13]0,
000776      [13]1,[13]0,
001000      [13]1,[13]0,
001002      [13]1,[13]0,
001004      [13]1,[13]0,
001006      [13]1,[13]0,
001010      [13]1,[13]0,
001012      [13]1,[13]0,[13]1;
001014      VOLTS1=-77E-3;VOLTS2=-210E-3;
001016      IFC=-100E-6;
001017      IPIN=4; CALL WTHRESH;
001021      SET F [13]0[34]1;
001022      SET D [34]1;
001023      SET F [34]0,[34]1,
001026      [34]0,[34]1,
001030      [34]0,[34]1,
001032      [34]0,[34]1,
001034      [34]0,[34]1,
001036      [34]0,[34]1,
001040      [34]0,[34]1,
001042      [34]0,[34]1;
001043      VOLTS1=-0.15; VOLTS2=-0.7;
001045      IPIN=16;CALL WTHRESH;
001047      SET F [10]0;
001050      SET F [34]0,[34]1,
001053      [34]0,[34]1,
001055      [34]0,[34]1,
001057      [34]0,[34]1,
001061      [34]0,[34]1,
001063      [34]0,[34]1,
001065      [34]0,[34]1,
001067      [34]0,[34]1,
001071      [34]0,[34]1,
001073      [34]0,[34]1;
001074      VOLTS=-0.55;
001075      IFC=0;
```

Figure 4-5. (Cont.)

```
001076      IPIN=15;CALL THRESHMAX;
001100      SET F [10]1;
001101      SET F [34]0,[34]1,
001104      [34]0,[34]1,
001106      [34]0,[34]1,
001110      [34]0,[34]1,
001112      [34]0,[34]1,
001114      [34]0,[34]1;
001115      IPIN=14;CALL THRESHMAX;
001117      SET F [34]0,[13]1;
001121      SET F [13]0,[13]1,
001124      [13]0,[13]1;
001125      IFC=-100E-6;
001126      IPIN=8;CALL WTHRESH;
001130      GOTO ABORT;
001131
001131      SUBR WTHRESH;
001131      SET PMU SENSE, RNG2;
001132      CPMU PIN IPIN;
001133      SET DELAY 20E-3, DC;
001134      FORCE CURRENT IFC,RNG1;
001135      ENABLE DCT1 GT VOLTS1;
001136      ENABLE DCT0 LT VOLTS2;
001137      MEASURE VALUE;
001140      FORCE PMU 0;
001141      END;
001141
001141      SUBR WLEAK;
001141      SET PMU SENSE, RNG1;
001142      CPMU PIN IPIN;
001143      SET DELAY 20E-3, DC;
001144      FORCE VOLTAGE VF;
001145      ENABLE DCT1 GT LEAK1;
001146      ENABLE DCT0 LT LEAK2;
001147      MEASURE VALUE;
001150      FORCE PMU 0;
001151      XPMU PIN;
001152      END;
001152
001152      SUBR NLEAK;
001152      DISABLE DCT1;
001153      SET PMU SENSE, RNG0;
001154      CPMU PIN IPIN;
001155      SET DELAY 100E-3, DC;
001156      FORCE VOLTAGE VF;
001157      ENABLE DCT0 LT LEAKAGE;
001160      MEASURE VALUE;
001161      FORCE PMU 0;
001162      XPMU PIN;
001163      END;
001163
001163      SUBR ZLEAK;
001163      DISABLE DCT1;
001164      SET PMU SENSE, RNG1;
```

Figure 4-5. (Cont.)

```
001165      CPMU PIN IPIN;
001166      SET DELAY 20E-3, DC;
001167      FORCE VOLTAGE VF;
001170      ENABLE DCT0 LT LEAKAGE;
001171      MEASURE VALUE;
001172      FORCE PMU 0;
001173      XPMU PIN;
001174      END;
001174
001174      SUBR THRESHMIN;
001174      DISABLE DCT1;
001175      SET PMU SENSE, RNG2;
001176      CPMU PIN IPIN;
001177      SET DELAY 20E-3, DC;
001200      FORCE CURRENT IFC, RNG1;
001201      ENABLE DCT0 GT VOLTS;
001202      MEASURE VALUE;
001203      FORCE PMU 0;
001204      XPMU PIN;
001205      END;
001205
001205      SUBR THRESHMAX;
001205      DISABLE DCT1;
001206      SET PMU SENSE, RNG2;
001207      CPMU PIN IPIN;
001210      SET DELAY 20E-3, DC;
001211      FORCE CURRENT IFC, RNG1;
001212      ENABLE DCT0 LT VOLTS;
001213      MEASURE VALUE;
001214      FORCE PMU 0;
001215      XPMU PIN;
001216      END;
001216
001216      SUBR YLEAK;
001216      DISABLE DCT1;
001217      SET PMU SENSE, RNG2;
001220      CPMU PIN IPIN;
001221      SET DELAY 20E-3, DC;
001222      FORCE VOLTAGE VF;
001223      ENABLE DCT0 LT LEAKAGE;
001224      MEASURE VALUE;
001225      FORCE PMU 0;
001226      XPMU PIN;
001227      END;
001227
001227      MSSAGE:  WRITE 'ATTACHED LINES EQUAL OPEN PINS (1) REFERENC
001230      ABORT:   END;
*
```

Figure 4-5. (Cont.)

FAIRCHILD
SYSTEMS TECHNOLOGY
464 E. Arques Ave., Sunnyvale, Calif. 94086

INTERNAL CORRESPONDENCE

March 2, 1971

To: FST-1/S-400 USERS

From: J. Burnett

Subject: RECOVERY AFTER CR ERRORS

When a feed check or read error occurs on the Card Reader and you are operating with DOPSY-5 software, the TTY bell will ring continuously to draw your attention to the error. The following procedure should be used for recovery:

1) STOP the card reader. This will turn off the bell and immediately you will feel much better.

2) Correct the error, i.e., for feed check, straighten the cards or for other errors correct the top card in the lower hopper and replace it in the upper hopper.

3) START the card reader. It should immediately go ready and begin once more to read cards.

J. Burnett

JB/nr